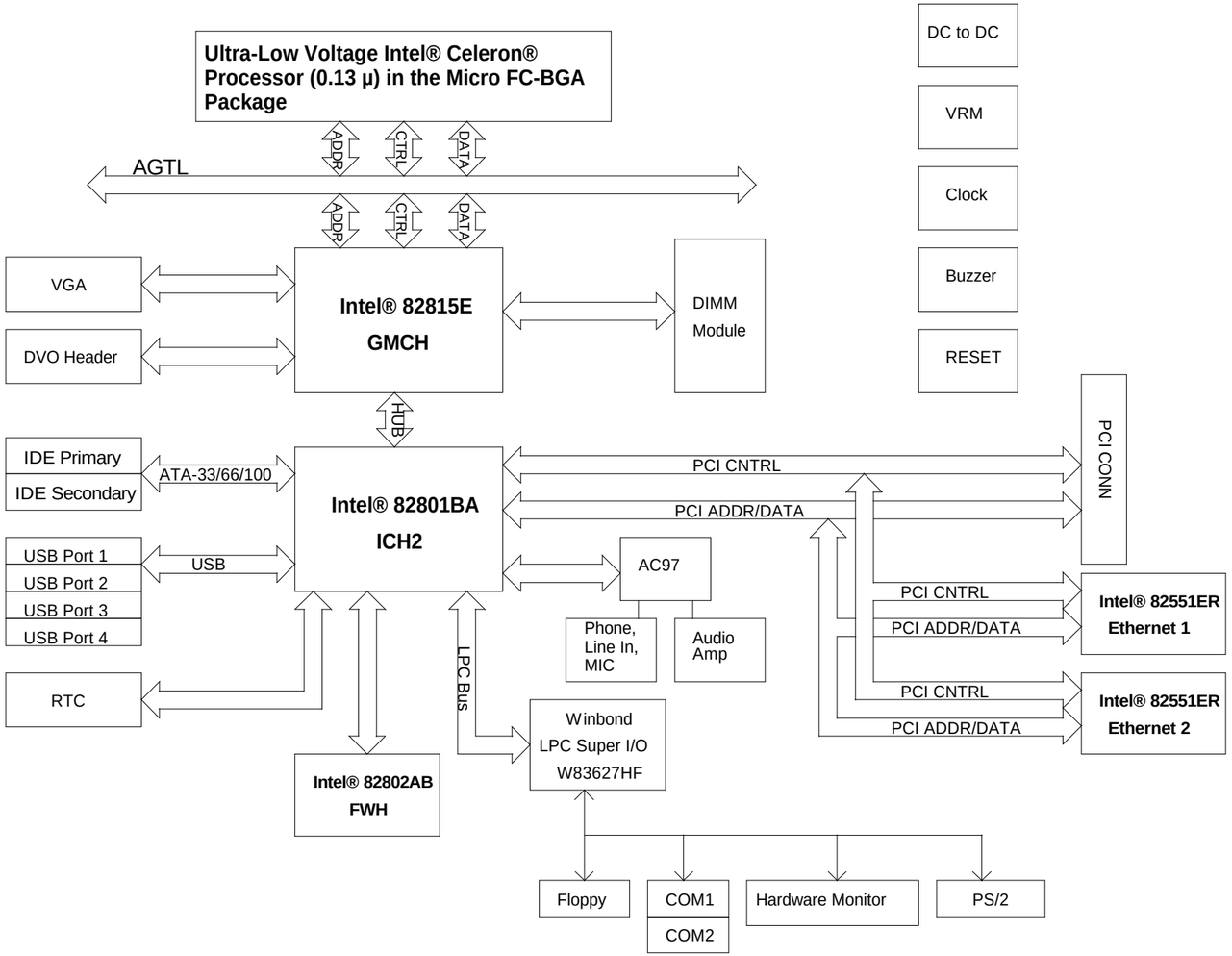
Intel® 815E Interactive Client Reference Design
Block Diagram



MANUFACTURING OPTIONS (Opt = XX):
CA = Communications Appliance Only
IC = Interactive Client Only

Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226

Title	BLOCK DIAGRAM	
Size A2	Document Number Intel® 815E Interactive Client Reference Design	Rev 1.1
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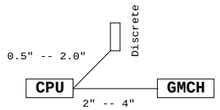
General Board Design Requirements

>> Board material shall be FR-4.
>> Right angle traces shall not be used.
>> Vias for decoupling capacitors shall be kept as close as possible to the capacitor pad.
>> Trace impedance shall be 60 ohms, +/- 15%
>> Total board thickness shall be .062".
>> GND layers shall not be split.
>> Top and bottom (outer) layers shall be no less than 1/2 oz copper before plating, inner layers shall be 1 oz copper.
>> Series terminating resistors shall be kept as close to the driving pin as possible.
>> Daisy chain signals going to more than one point shall not use stubs.
>> Unless otherwise noted, all signal traces shall be between 5 and 6 mil width.
>> Unless otherwise noted, minimum space between traces shall be 10 mils, including adjacent layers.
>> One registration target shall be included on each corner of the board.
>> Other specific routing requirements are included throughout schematic sheets.

CPU Routing Requirements



>> Route all GTL traces between CPU and GMCH as shown in the diagram to the right.
>> Route all traces between CPU and GMCH on a layer adjacent to a ground plane, without layer changes.
>> Minimum space between traces shall be 10 mils (unless otherwise noted); this includes adjacent signal layers.
>> Minimum space between traces may be reduced to 5 mils when breaking out of a footprint. The total length of trace routed using 5 mil spacing shall be less than 250 mils.
>> The following signals require 25 mil spacing from other traces, including adjacent layers:

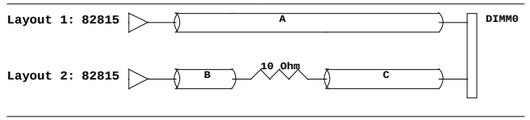
HA#[31:3], HD#[63:0], BREQ#0, HADS#, BNR#, BPRI#, HLOCK#, DEFER#, HTRDY#, DBSY#, DRDY#, HIT#, HITM#, A20M#, IGNNE#, INIT#, INTR, NMI, PWR_OK_2P5, SMI#, CPUSLP#, STPCLK#, 66#/100SEL,100#/133SEL,FERR#,CPURST#, HREQ#[4:0], RS#[2:0], GTLREF[7:0], PLL[2:1], (CPU_TCK/TMS/TDI/TDO/TRST#, PRDY#, PREQ#).

>> AGTL signals shall be well isolated from system memory signals. AGTL signal trace edges shall be at least 30 mils from system memory trace edges within 100 mils of the ball of the 82815 GMCH.
>> Route GTLREF using 25 mil minimum width trace, and separate from all other traces by 25 mils minimum.
>> Route PLL[2:1] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum.

Memory Bus Routing Requirements

>> Minimum space between memory traces and other types of traces is 30 mils, including adjacent signal layers.
>> Memory address, data, and control lines shall be routed as separate groups and treated as different signal types.

Topologies



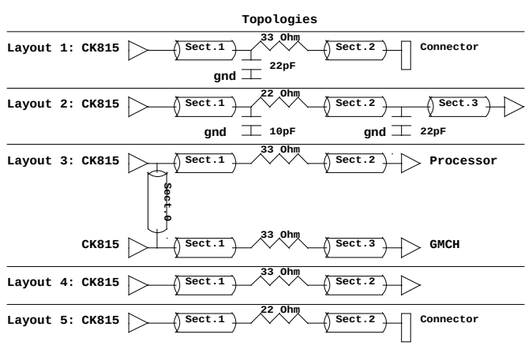
Routing Solution :

Signal	Topologies	Width (mils)	Spacing (mils)	A (inches)	B (inches)	C (inches)
SM_CSA#[1..0]	Layout 1	5	10	1-4.5		
SM_MAA[7:4]	Layout 2	10	10		0.4-0.5	2-4
SM_CKE[1:0]	Layout 1	10	10	3-4		
SM_MD[63:0]	Layout 1	5	10	1.75-4		
SM_DQMA[7:0]	Layout 1	10	10	1.5-3.5		
SM_CAS#, SM_RAS#, SM_WE#	Layout 1	10	10	1-4.0		
SM_BS[1:0], SM_MAA[12:8], [3:0]	Layout 1	10	10	1-4.0		

Clock Routing Requirements

>> Clock traces shall not alternate layers.
>> All clocks shall be routed 5 mils wide with 15 mil spacing to any other signals.
>> It is recommended to place capacitor sites within 0.5 inches of the receiver of all clocks. They are useful in system debug and AC tuning.
>> Series resistor for clock guidelines: 22 ohm for GMCH SCLK and SDRAM clocks. All other clocks use 33 ohm.
>> Each DIMM clock shall be matched within ±10 mils.

Topologies



Routing Solution : **Note : A < 6"**

Destination	Topologies	Sect.0	Sect.1	Sect.2	Sect.3
MEMCLK[3..0]	Layout 5	N/A	<0.5"	A	N/A
DCLK_WR	Layout 2	N/A	<0.5"=L1	A+3.5"-L1	0.5"
CPUHCLK	Layout 3	<0.1"	<0.5"	A+5.2"	N/A
GMCHHCLK			<0.5"		
GMCH_3V66	Layout 4	N/A	<0.5"	A+8"	N/A
ICH_3V66	Layout 4	N/A	<0.5"	A+8"	N/A
PCLKICH	Layout 4	N/A	<0.5"	A+8"	N/A
PCLK559A,B; PCLKFWH ; PCLKSIO	Layout 4	N/A	<0.5"	A+8.5" to A+14"	N/A
PCICLKA	Layout 1	N/A	<0.5"	A+5" to A+11"	N/A

PCI Bus Routing Requirements

PCI Bus GROUPS

>> Address/Data Signals: AD[31:0]
>> Control Signals:

C/BE[3:0]#, REQ[4:1]#, GNT[4:1]#, INT[A:D]#, PCIRST#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PERR#, PAR, LOCK#

Hub Interface Routing Requirements

>> Hub interface data signals shall be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals may be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH and the ICH2, the hub interface data signals may be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals shall be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH/ICH2 components.
>> The maximum trace length for the hub interface data signals is 8 inches. These signals shall each be matched within 0.1 inch of the HLSTB and HLSTB# signals.
>> HL[10:0] should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals may be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. The maximum trace length for the hub interface data signals is 7". These signals shall each be matched within .1"" of the HLSTB and HLSTB# signals.

HUB Bus GROUPS

>> Address/Data Signals: HL[10:0]
>> Control Signals: HLSTB, HLSTB# (differential strobe pair).

DVO Interface Routing Requirements

>> Route data signals (LTVDATA[11:0]) with a trace width of 5 mils and a trace spacing of 20 mils. These signals may be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes.
>> To break out of the GMCH, the DVO data signals may be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals shall be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH component. The maximum trace length for the DVO data signals is 7 inches. These signals shall each be matched within 0.1 inch of the LTVCLKOUT[1] and LTVCLKOUT[0] signals.
>> Route the LTVCLKOUT[1:0] signals 5 mils wide and 20 mils apart. This signal pair shall be a minimum of 20 mils from any adjacent signals. The maximum length for LTVCLKOUT[1:0] is 7 inches and the two signals shall be the same length.

AC97 Interface Routing Requirements

>> To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.
>> Special consideration must be given for the ground return paths for the analog signals.
>> Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals shall be located as far as possible from each other.
>> Partition the board with all analog components grouped together in one area and all digital components in another.
>> Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
>> Keep digital signal traces, especially the clocks, as far as possible from the analog input and voltage reference pins.
>> Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
>> Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which could cause a ground loop, thereby greatly increasing EMI issues and degrading the analog and digital signal quality.
>> Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
>> All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
>> Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
>> Locate the crystal or oscillator close to the codec.

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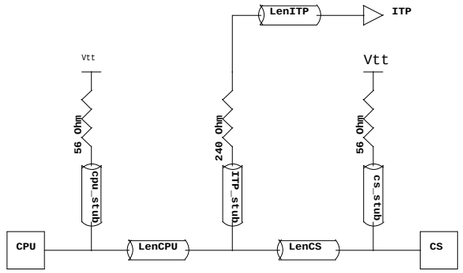
Power Supply Routing Requirements

>> All unrelated signals and power planes shall be kept away from the switching circuits, devices, magnetics, and traces.

>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.

>> Refer to the power supply data sheets and the schematic sheets for more detail.

RESET#/RESET2# Routing Requirements



Routing Solution :

Parameter	Minimum (in)	Maximum (in)
LenCS	0.5	1.5
LenITP	1	3
LenCPU	0.5	1.5
cs stub	0.5	1
cpu stub	0.5	1
ITP stub	short as possible	

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Title: LAYOUT NOTES 2

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U1A

VCORE

D[63:0]

VCCVID1 VCCVID2 VCCVID3 VCCVID4 VCCVID5 VCCVID6 VCCVID7 VCCVID8 VCCVID9 VCCVID10 VCCVID11 VCCVID12 VCCVID13 VCCVID14 VCCVID15 VCCVID16 VCCVID17 VCCVID18 VCCVID19 VCCVID20 VCCVID21 VCCVID22 VCCVID23 VCCVID24 VCCVID25 VCCVID26 VCCVID27 VCCVID28 VCCVID29 VCCVID30 VCCVID31 VCCVID32 VCCVID33 VCCVID34 VCCVID35 VCCVID36 VCCVID37 VCCVID38 VCCVID39 VCCVID40 VCCVID41 VCCVID42 VCCVID43 VCCVID44 VCCVID45 VCCVID46 VCCVID47 VCCVID48 VCCVID49 VCCVID50 VCCVID51 VCCVID52 VCCVID53 VCCVID54 VCCVID55 VCCVID56 VCCVID57 VCCVID58 VCCVID59 VCCVID60 VCCVID61 VCCVID62 VCCVID63 VCCVID64 VCCVID65 VCCVID66 VCCVID67 VCCVID68 VCCVID69 VCCVID70 VCCVID71 VCCVID72 VCCVID73 VCCVID74 VCCVID75 VCCVID76 VCCVID77 VCCVID78 VCCVID79 VCCVID80 VCCVID81

8 HD#[63:0]

HD#0	A16	HD#0
HD#1	B17	HD#1
HD#2	A17	HD#2
HD#3	D23	HD#3
HD#4	B19	HD#4
HD#5	C20	HD#5
HD#6	C16	HD#6
HD#7	A20	HD#7
HD#8	A22	HD#8
HD#9	A19	HD#9
HD#10	A23	HD#10
HD#11	A24	HD#11
HD#12	C18	HD#12
HD#13	D24	HD#13
HD#14	B24	HD#14
HD#15	A18	HD#15
HD#16	E23	HD#16
HD#17	B21	HD#17
HD#18	B23	HD#18
HD#19	E26	HD#19
HD#20	C24	HD#20
HD#21	F24	HD#21
HD#22	D25	HD#22
HD#23	E24	HD#23
HD#24	B25	HD#24
HD#25	G24	HD#25
HD#26	H24	HD#26
HD#27	F26	HD#27
HD#28	L24	HD#28
HD#29	H25	HD#29
HD#30	C26	HD#30
HD#31	K24	HD#31
HD#32	G26	HD#32
HD#33	K25	HD#33
HD#34	J24	HD#34
HD#35	K26	HD#35
HD#36	F25	HD#36
HD#37	N26	HD#37
HD#38	J26	HD#38
HD#39	M24	HD#39
HD#40	U26	HD#40
HD#41	P25	HD#41
HD#42	L26	HD#42
HD#43	R24	HD#43
HD#44	R26	HD#44
HD#45	M25	HD#45
HD#46	V25	HD#46
HD#47	T24	HD#47
HD#48	M26	HD#48
HD#49	P24	HD#49
HD#50	AA26	HD#50
HD#51	T26	HD#51
HD#52	U24	HD#52
HD#53	Y25	HD#53
HD#54	W26	HD#54
HD#55	V26	HD#55
HD#56	AB25	HD#56
HD#57	T25	HD#57
HD#58	Y24	HD#58
HD#59	W24	HD#59
HD#60	Y26	HD#60
HD#61	AB24	HD#61
HD#62	AA24	HD#62
HD#63	V24	HD#63

uFCBGA

HA#[31:3] 8

HA#3	K1	HA#3
HA#4	J1	HA#4
HA#5	G2	HA#5
HA#6	K3	HA#6
HA#7	J2	HA#7
HA#8	H3	HA#8
HA#9	G1	HA#9
HA#10	A3	HA#10
HA#11	J3	HA#11
HA#12	H1	HA#12
HA#13	D3	HA#13
HA#14	F3	HA#14
HA#15	G3	HA#15
HA#16	C2	HA#16
HA#17	B5	HA#17
HA#18	B11	HA#18
HA#19	C6	HA#19
HA#20	B9	HA#20
HA#21	B7	HA#21
HA#22	C8	HA#22
HA#23	A8	HA#23
HA#24	A10	HA#24
HA#25	B3	HA#25
HA#26	A13	HA#26
HA#27	A9	HA#27
HA#28	C3	HA#28
HA#29	C12	HA#29
HA#30	C10	HA#30
HA#31	A6	HA#31
HA#32	A15	
HA#33	A14	
HA#34	B13	
HA#35	A12	

VID[4:0] 15,27

VID0	AB1	VID0
VID1	AC2	VID1
VID2	AE2	VID2
VID3	AF3	VID3
GND/VID4	R3	VID4

HREQ#[4:0] 8

REQ#0	R1	HREQ#0
REQ#1	L3	HREQ#1
REQ#2	T1	HREQ#2
REQ#3	U1	HREQ#3
REQ#4	L1	HREQ#4

DEP0#	AE24
DEP1#	AD25
DEP2#	AE25
DEP3#	AC24
DEP4#	AF24
DEP5#	AD26
DEP6#	AC26
DEP7#	AD24

RS#[2:0] 8

RS#2	U3	RS#2
RS#1	V1	RS#1
RS#0	Y3	RS#0

VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9 VTT10 VTT11 VTT12 VTT13 VTT14 VTT15 VTT16 VTT17 VTT18 VTT19 VTT20 VTT21 VTT22 VTT23 VTT24 VTT25 VTT26 VTT27 VTT28 VTT29 VTT30 VTT31 VTT32 VTT33 VTT34 VTT35 VTT36 VTT37 VTT38

J4 J23 L4 L23 N23 R23 U23 V4 W23 AA4 AA23 AC4 AC23 AD6 AD8 AD12 AD14 AD18 AD20 AE3 AE18 AE1 AE2 G23 G4 E6 E4 D5 C21 C19 C17 C15 C13 C11 C9 C7 C5 A26

VTT

NOTE:
PLACE ALL COMPONENTS FOR BOTH
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Title	uFCBGA PART 1	
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GTLREF Generation Circuit
Use 0603 Packages and distribute
within 500 mils of uFCPGA
GTLREF Inputs (1 cap for every 2 inputs).

Route trace as wide as possible

Place 0603 cap. near VCMOS Processor Pin

CMOSREF generation

CPU THRMDP and THRMDN are routed in parallel and on the same layer.

Keep these traces as close as possible and away from other signals (>=20 mils spacing)

>> Keep components close to PLL1 and PLL2. Trace widths must be 20 mil minimum. Trace resistance should be 1 ohm.

NEAR uFCBGA

Close to uFCBGA

NOTE:
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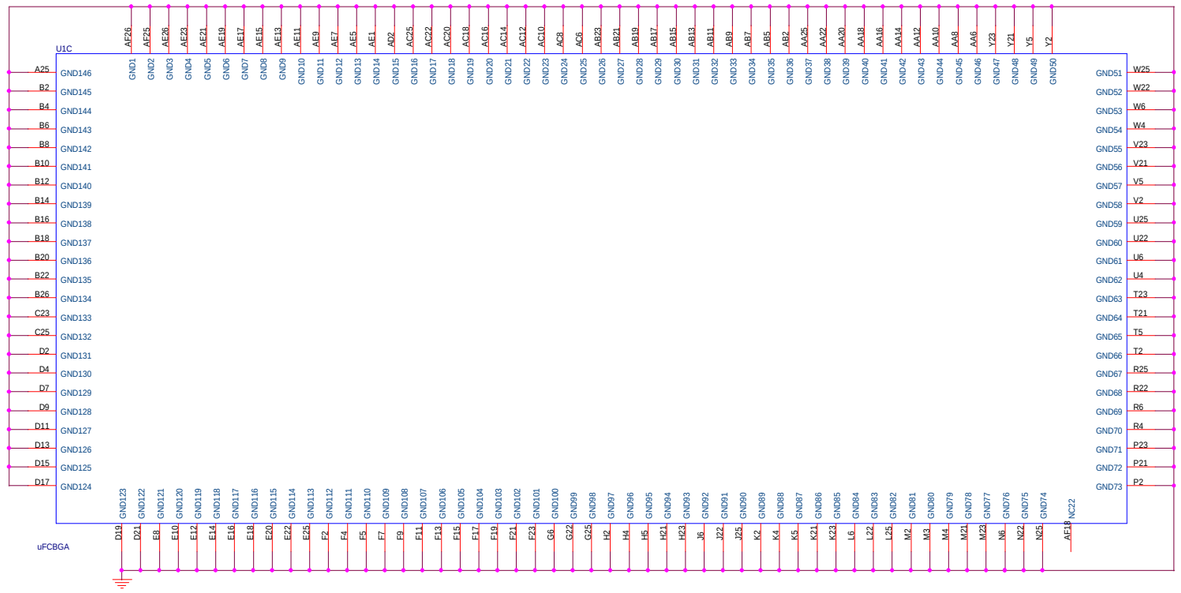

VCORE

Distribute directly under uFCBGA near pin/ball

C12 0.22U/10V 10% 0603 Panasonic
C13 0.22U/10V 10% 0603 Panasonic
C14 0.22U/10V 10% 0603 Panasonic
C15 0.22U/10V 10% 0603 Panasonic
C16 0.22U/10V 10% 0603 Panasonic
C17 0.22U/10V 10% 0603 Panasonic
C18 0.22U/10V 10% 0603 Panasonic
C19 0.22U/10V 10% 0603 Panasonic
C20 0.22U/10V 10% 0603 Panasonic
C21 0.22U/10V 10% 0603 Panasonic
C22 0.22U/10V 10% 0603 Panasonic
C23 0.22U/10V 10% 0603 Panasonic
C24 0.22U/10V 10% 0603 Panasonic
C25 0.22U/10V 10% 0603 Panasonic
C26 0.22U/10V 10% 0603 Panasonic
C27 0.22U/10V 10% 0603 Panasonic
C28 0.22U/10V 10% 0603 Panasonic
C29 0.22U/10V 10% 0603 Panasonic
C30 0.22U/10V 10% 0603 Panasonic
C31 0.22U/10V 10% 0603 Panasonic
C32 0.22U/10V 10% 0603 Panasonic
C33 0.22U/10V 10% 0603 Panasonic
C34 0.22U/10V 10% 0603 Panasonic
C35 0.22U/10V 10% 0603 Panasonic

VCORE

Distribute around package periphery

C36 10U/6.3V 10% 1206 AVX
C37 10U/6.3V 10% 1206 AVX
C38 10U/6.3V 10% 1206 AVX
C39 10U/6.3V 10% 1206 AVX
C40 10U/6.3V 10% 1206 AVX
C41 10U/6.3V 10% 1206 AVX
C42 10U/6.3V 10% 1206 AVX
C43 10U/6.3V 10% 1206 AVX
C44 10U/6.3V 10% 1206 AVX
C45 10U/6.3V 10% 1206 AVX

NOTE:
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Title: uFCBGA PART 3

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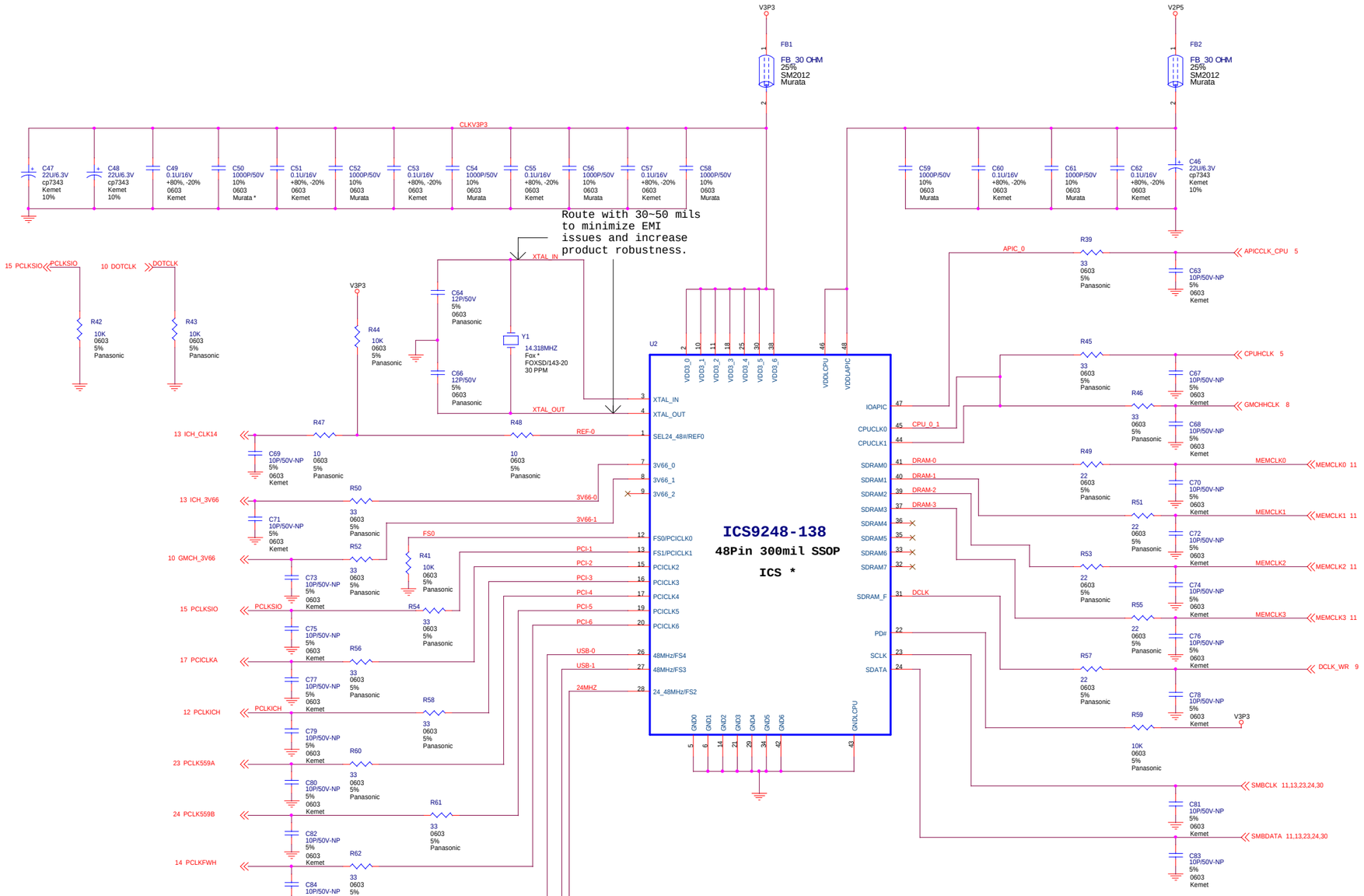

FS3	FS2	CPU MHz	SDRAM MHz
0	0	66	100
0	1	100	100
1	0	133	133
1	1	100	100

Note : 1 --> High ; 0 --> Low
BIOS will assign SDRAM memory clock when FSB is 133MHz

NOTE:
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Title: CLOCK SYNTHESIZER

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Place as close as possible to GMCH

VTT

R68 63.4 1% 0603 Panasonic

If A-2 stepping is used, populate with 75 ohm, 1% resistor (ERJ-3EKF75R0V). A-2 stepping = VTT*2/3, others = VTT * 0.7

GMCHGTLREF

R69 150 1% 0603 Panasonic

C91 0.1U/16V +80%, -20% 0603 Kemet

C92 0.1U/16V +80%, -20% 0603 Kemet

Route trace as wide as possible

V1P8

L2 0.022U 10% API Delevan

C88 33U/20V cp7343 AVX 20%

C89 0.1U/16V +80%, -20% 0603 Kemet

C90 0.01U/50V +80%, -20% 0402 Panasonic

U3A

VCC1_8[0] W6
VCC1_8[1] V9
VCC1_8[2] Y18
VCC1_8[3] AA6
VCC1_8[4] AA8
VCC1_8[5] AA11
VCC1_8[6] AA13
VCC1_8[7] AA15
VCC1_8[8] AA17
VCC1_8[9] AA19
VCC1_8[10] AB16
VCC1_8[11] AB20
VCC1_8[12] AC22
VCC1_8[13] AD19
VCC1_8[14] C25
VCC1_8[15] E24
VCC1_8[16] F23
VCC1_8[17] G22
Vccdpll_VCC1_8[18] J7
VCC1_8[19] K6
VCC1_8[20] M6
VCC1_8[21] P6
VCC1_8[22] T6
VCC1_8[23] V7
VCC1_8[24] G26
VCC1_8[25] Y7
Vccda_VCC1_8[26] AA21
Vccha_VCC1_8[27] E23
Vccdaca2_VCC1_8[28] AE26
Vccdaca2_VCC1_8[29] AF25

DEBUG: Place within 150 mils of GMCH and as close as possible to ADS#

R70 56.2-NP 1% 0603 Panasonic

R71 56.2 1% 0603 Panasonic

7 GMCHHCLK

C93 18P/50V-NP 5% 0603 Panasonic

Do not stuff. Place site within 0.5" of clock ball (AA7)

	U6	GTLREFA
	AA10	GTLREFB
	AA7	HTCLK
14,15,22,30 PCIRST_GMCH#	H3	RESET#
5 CPURST#	AA5	CPURST#
5 HLOCK#	L4	HLOCK#
5 DEFER#	M3	DEFER#
5 HADS#	G1	ADS#
5 BNR#	N4	BNR#
5 BPRI#	M5	BPRI#
5 DBSY#	J3	DBSY#
5 DRDY#	J1	DRDY#
5 HIT#	K1	HIT#
5 HITM#	L3	HITM#
5 HTRDY#	K3	HTRDY#

4 HA#[31:3]

HA#3	R4	HA3#
HA#4	P1	HA4#
HA#5	T2	HA5#
HA#6	R3	HA6#
HA#7	N5	HA7#
HA#8	P5	HA8#
HA#9	R1	HA9#
HA#10	U1	HA10#
HA#11	P2	HA11#
HA#12	T1	HA12#
HA#13	T3	HA13#
HA#14	P3	HA14#
HA#15	T5	HA15#
HA#16	R5	HA16#
HA#17	V5	HA17#
HA#18	Y2	HA18#
HA#19	V3	HA19#
HA#20	W1	HA20#
HA#21	U4	HA21#
HA#22	V2	HA22#
HA#23	W3	HA23#
HA#24	W4	HA24#
HA#25	U5	HA25#
HA#26	Y5	HA26#
HA#27	Y3	HA27#
HA#28	U3	HA28#
HA#29	Y1	HA29#
HA#30	W5	HA30#
HA#31	V1	HA31#

4 HREQ#[4:0]

HREQ#0	M1	HREQ0#
HREQ#1	N1	HREQ1#
HREQ#2	M2	HREQ2#
HREQ#3	L5	HREQ3#
HREQ#4	N3	HREQ4#

4 RS#[2:0]

RS#0	K2	RS0#
RS#1	L1	RS1#
RS#2	H1	RS2#

VSS[0] B26
VSS[1] C3
VSS[2] C6
VSS[3] C9
VSS[4] C12
VSS[5] C15
VSS[6] C18
VSS[7] C21
VSS[8] C24
VSS[9] D1
VSS[10] E5
VSS[11] E7
VSS[12] E10
VSS[13] E12
VSS[14] E15
VSS[15] E17
VSS[16] E20
VSS[17]_Vssba E22
VSS[18] F1
VSS[19] F3
VSS[20] F11
VSS[21] F13
VSS[22] F16
VSS[23] F25
VSS[24] G9
VSS[25] G17
VSS[26] G21
VSS[27] G23
VSS[28] H6
VSS[29] H22
VSS[30] J2
VSS[31] J5
VSS[32] J23
VSS[33] J25
VSS[34] K4
VSS[35]_Vssdpll K7

815E GMCH

544 mBGA

PART1

HOST INTERFACE

HD0#	AA1	HD#0
HD1#	AB2	HD#1
HD2#	AF2	HD#2
HD3#	AD4	HD#3
HD4#	AB1	HD#4
HD5#	AB3	HD#5
HD6#	AA3	HD#6
HD7#	AC4	HD#7
HD8#	AC1	HD#8
HD9#	AF3	HD#9
HD10#	AD1	HD#10
HD11#	AE3	HD#11
HD12#	AD2	HD#12
HD13#	AD3	HD#13
HD14#	AF1	HD#14
HD15#	AA4	HD#15
HD16#	AD6	HD#16
HD17#	AC3	HD#17
HD18#	AE1	HD#18
HD19#	AB6	HD#19
HD20#	AF4	HD#20
HD21#	AE5	HD#21
HD22#	AC8	HD#22
HD23#	AB5	HD#23
HD24#	AF5	HD#24
HD25#	AC6	HD#25
HD26#	AF6	HD#26
HD27#	AD11	HD#27
HD28#	AF8	HD#28
HD29#	AD8	HD#29
HD30#	AD5	HD#30
HD31#	AB7	HD#31
HD32#	AF7	HD#32
HD33#	AD7	HD#33
HD34#	AB8	HD#34
HD35#	AE7	HD#35
HD36#	AE9	HD#36
HD37#	AB9	HD#37
HD38#	AF9	HD#38
HD39#	AD10	HD#39
HD40#	AF12	HD#40
HD41#	AB11	HD#41
HD42#	AB10	HD#42
HD43#	AD9	HD#43
HD44#	AC10	HD#44
HD45#	AE10	HD#45
HD46#	AD14	HD#46
HD47#	AD12	HD#47
HD48#	AB12	HD#48
HD49#	AE11	HD#49
HD50#	AE15	HD#50
HD51#	AF11	HD#51
HD52#	AF13	HD#52
HD53#	AB14	HD#53
HD54#	AF14	HD#54
HD55#	AB13	HD#55
HD56#	AB15	HD#56
HD57#	AE13	HD#57
HD58#	AC14	HD#58
HD59#	AD13	HD#59
HD60#	AD15	HD#60
HD61#	AF16	HD#61
HD62#	AF15	HD#62
HD63#	AC12	HD#63

HD#[63:0] 4

NOTE:
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Title: GMCH PART 1

Size: A2 | Document Number: Intel® 815E Interactive Client Reference Design | Rev: 1.1

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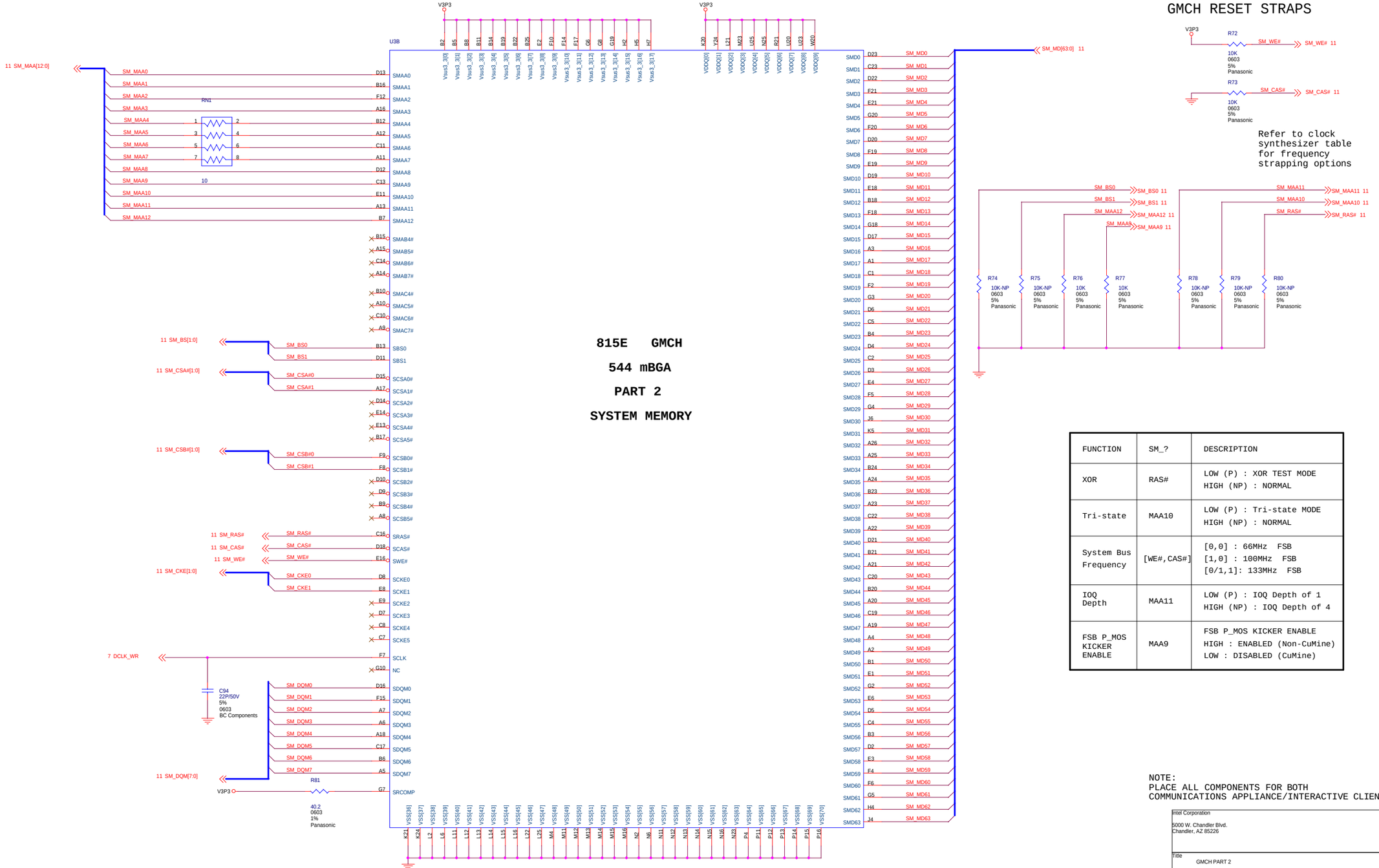
815E GMCH
544 mBGA
PART 2
SYSTEM MEMORY



GMCH RESET STRAPS

Refer to clock synthesizer table for frequency strapping options

FUNCTION	SM_?	DESCRIPTION
XOR	RAS#	LOW (P) : XOR TEST MODE HIGH (NP) : NORMAL
Tri-state	MAA10	LOW (P) : Tri-state MODE HIGH (NP) : NORMAL
System Bus Frequency	[WE#,CAS#]	[0,0] : 66MHz FSB [1,0] : 100MHz FSB [0/1,1]: 133MHz FSB
IOQ Depth	MAA11	LOW (P) : IOQ Depth of 1 HIGH (NP) : IOQ Depth of 4
FSB P_MOS KICKER ENABLE	MAA9	FSB P_MOS KICKER ENABLE HIGH : ENABLED (Non-CuMine) LOW : DISABLED (CuMine)

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815E GMCH

544 mBGA

PART3
DISPLAY CACHE, VIDEO, AND HUB INTERFACE

U3C

DISPLAY CACHE

VIDEO DIGITAL OUT INTERFACE

GRAPHICS INTERFACE

HUB I/F

AGP

J2

HEADER 6X2_2MM

Samtec *

G1--G8 are the Vias on the tooling hole

DO NOT STUFF
Place site w / in 0.5" of clock ball (AE24)

Place within 0.5" of the GMCH Ball

Place as close as possible to GMCH and via straight to VSS plane

Place as close as possible to GMCH

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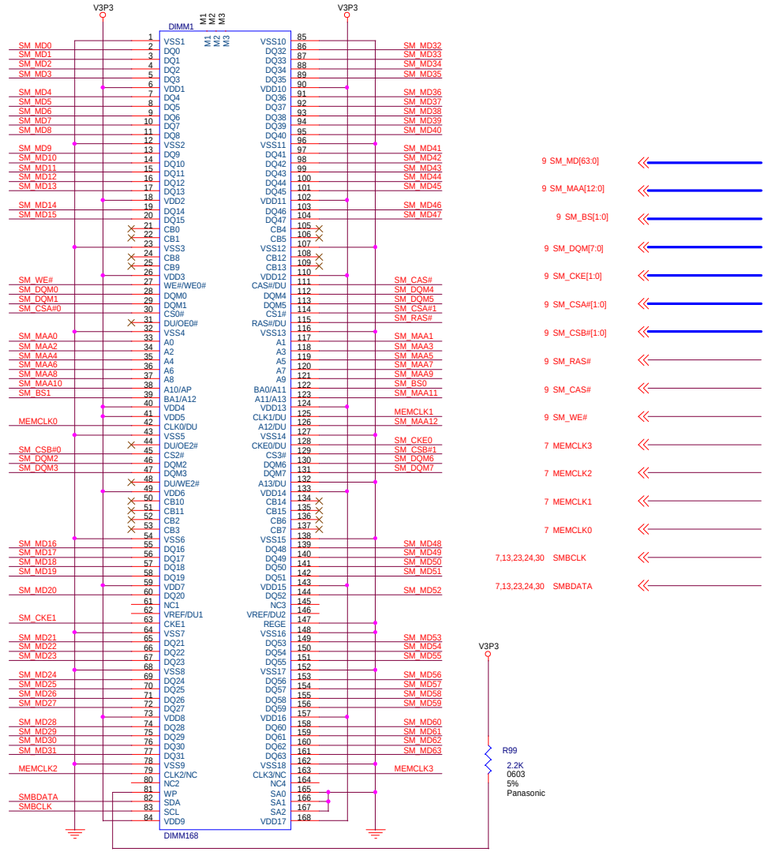

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ICH2

360 EBGA

PART1

U4A

V3P3 V3P3 V1P8 V1P8

VCC3_3[0] R5 · VCC3_3[1] T5 · VCC3_3[2] U5 · VCC3_3[3] V5 · VCC3_3[4] V6 · VCC3_3[5] V7 · VCC3_3[6] V8 · VCC3_3[7] R18 · VCC3_3[8] P18 · VCC3_3[9] J18 · VCC3_3[10] H18 · VCC3_3[11] G18 · VCC3_3[12] F18 · VCC3_3[13] E18 · VCC3_3[14] E17 · VCC3_3[15] E16 · VCC3_3[16] E15 · VCC3_3[17] E14

VCCSUS3_3[0] F5 · VCCSUS3_3[1] G5 · VCCSUS3_3[2] V17 · VCCSUS3_3[3] V18 · VCCSUS3_3[4] U18 · VCCSUS3_3[5] T18

VCC1_8[0] D2 · VCC1_8[1] E5 · VCC1_8[2] P5 · VCC1_8[3] V9 · VCC1_8[4] K19 · VCC1_8[5] L19 · VCC1_8[6] D10

VCCSUS1_8[0] H5 · VCCSUS1_8[1] J5 · VCCSUS1_8[2] V14 · VCCSUS1_8[3] V15 · VCCSUS1_8[4] V16

PCI

17,23,24 AD[31:0]

AD0 AA4 AD0 · AD1 AB4 AD1 · AD2 Y4 AD2 · AD3 W5 AD3 · AD4 W4 AD4 · AD5 Y5 AD5 · AD6 AB3 AD6 · AD7 AA5 AD7 · AD8 AB5 AD8 · AD9 Y3 AD9 · AD10 W6 AD10 · AD11 W3 AD11 · AD12 Y6 AD12 · AD13 Y2 AD13 · AD14 AA6 AD14 · AD15 Y1 AD15 · AD16 V2 AD16 · AD17 AA8 AD17 · AD18 V1 AD18 · AD19 AB8 AD19 · AD20 U4 AD20 · AD21 W9 AD21 · AD22 U3 AD22 · AD23 Y9 AD23 · AD24 U2 AD24 · AD25 AB9 AD25 · AD26 U1 AD26 · AD27 W10 AD27 · AD28 T4 AD28 · AD29 Y10 AD29 · AD30 T3 AD30 · AD31 AA10 AD31

17,23,24 C_BE#[3:0]

C_BE#0 AA3 C/BE0# · C_BE#1 AB6 C/BE1# · C_BE#2 Y8 C/BE2# · C_BE#3 AA9 C/BE3#

17,23,24,30 DEVSEL# AB7 DEVSEL#

17,23,24,30 FRAME# V3 FRAME#

17,23,24,30 IRDY# W8 IRDY#

17,23,24,30 TRDY# V4 TRDY#

17,23,24,30 STOP# W1 STOP#

17,23,24 PAR W2 PAR

30 ICHRST# AA15 PCIRST#

17,30 PLOCK# AA7 PLOCK#

17,23,24,30 SERR# W7 SERR#

17,23,24,30 PERR# Y7 PERR#

Y15 PME#

30 PCPCI_REQ#A M3 REQA#/GPIO0

L2 GNTA#/GPIO16

7 PCLKICH W11 PCICLK

C101 10P/50V-NP 5% 0603 Kemet

GPIO

30 ICH_IRQE# N3 PIRQE#

30 ICH_IRQF# N2 PIRQF#/GPIO3

30 ICH_IRQG# N1 PIRQG#/GPIO4

30 GPIO7 AA11 GPI7

30 GPIO8 Y14 GPI8

30 GPIO12 W14 GPI12

30 GPIO13 AB15 GPI13

A15 GPO18 · D14 GPO19 · C14 GPO20 · L1 GPO21 · B14 GPO22 · A14 GPO23 · AB14 GPO27 · AA14 GPO28

VSS_0 B10 · VSS_1 B8 · VSS_2 C9 · VSS_3 D9 · VSS_4 D8 · VSS_5 D7 · VSS_6 D6 · VSS_7 D5 · VSS_8 C4 · VSS_9 E6 · VSS_10 E7 · VSS_11 E8 · VSS_12 E9 · VSS_13 J9 · VSS_14 J10 · VSS_15 J11 · VSS_16 J12 · VSS_17 J13 · VSS_18 J14 · VSS_19 K9 · VSS_20 K10 · VSS_21 K11 · VSS_22 K12 · VSS_23 K13 · VSS_24 K14 · VSS_25 L9 · VSS_26 L10 · VSS_27 L11 · VSS_28 L12 · VSS_29 L13 · VSS_30 L14 · VSS_31 M9 · VSS_32 M10 · VSS_33 M11 · VSS_34 M12 · VSS_35 M13 · VSS_36 M14

CPU

A20M# D11 A20M# 5 · CPUSLP# A12 CPUSLP# 5 · FERR# R22 FERR# 5 · IGNNE# A11 IGNNE# 5 · INIT# C12 INIT# 5,14,30 · INTR C11 INTR 5 · NMI B11 NMI 5 · SMI# B12 SMI# 5 · STPCLK# C10 STPCLK# 5 · RCIN# B13 RCIN# 15,30 · A20GATE C13 A20GATE 15,30 · CPUPWRGD A13 PWR_OK_CPU 5

HUB

HL0 A4 HL0 · HL1 B5 HL1 · HL2 A5 HL2 · HL3 B6 HL3 · HL4 B7 HL4 · HL5 A8 HL5 · HL6 B8 HL6 · HL7 A9 HL7 · HL8 C8 HL8 · HL9 C6 HL9 · HL10 C7 HL10 · HL11 C5

HL[0..10] 10

RESV2PD

For Test/Debug R100 0-NP 0603 1% Panasonic

V1P8 R101 40.2 0603 1% Panasonic Place as close as possible to ICH2

HL_STB A6 HLSTB 10 · HL_STB# A7 HLSTB# 10

HLCOMP A3 IHCOMP_PU

HUBREF B4 ICH2HLREF

V1P8 Place as close as possible to ICH2 R102 301 0603 1% Panasonic · R103 301 0603 1% Panasonic · C100 0.1U/16V +80%, -20% 0603 Kemet

IRQ

PIRQA# P1 PIRQ#A 17,30 · PIRQB# P2 PIRQ#B 17,30 · PIRQC# P3 PIRQ#C 17,23,30 · PIRQD# N4 PIRQ#D 17,24,30

IRQ14 F21 IRQ14 18 · IRQ15 C16 IRQ15 18

APICCLK N20 · APICD0 P22 · APICD1 N19

SERIRQ N21 SERIRQ 15,30

R104 10K 0603 5% Panasonic · R105 10K 0603 5% Panasonic

PCI

REQ0 R2 PREQ#0 17,30 · REQ1 R3 PREQ#1 23,30 · REQ2 T1 PREQ#2 24,30 · REQ3 AB10 PREQ#3 30 · REQ4 P4 PREQ#4 30 · REQB#/REQ5#/GPIO1 L3 PREQ#5 30

GNT0 M2 PGNT#0 17 · GNT1 M1 PGNT#1 23 · GNT2 R4 PGNT#2 24 · GNT3 T2 · GNT4 R1 · GNTB#/GNT5#/GPIO17 L4

LAN

LAN_RXD0 G2 · LAN_RXD1 G1 · LAN_RXD2 H1 · LAN_TXD0 F3 · LAN_TXD1 F2 · LAN_TXD2 F1

LAN_CLK G3 · LAN_RSTSYNC H2

NOTE:
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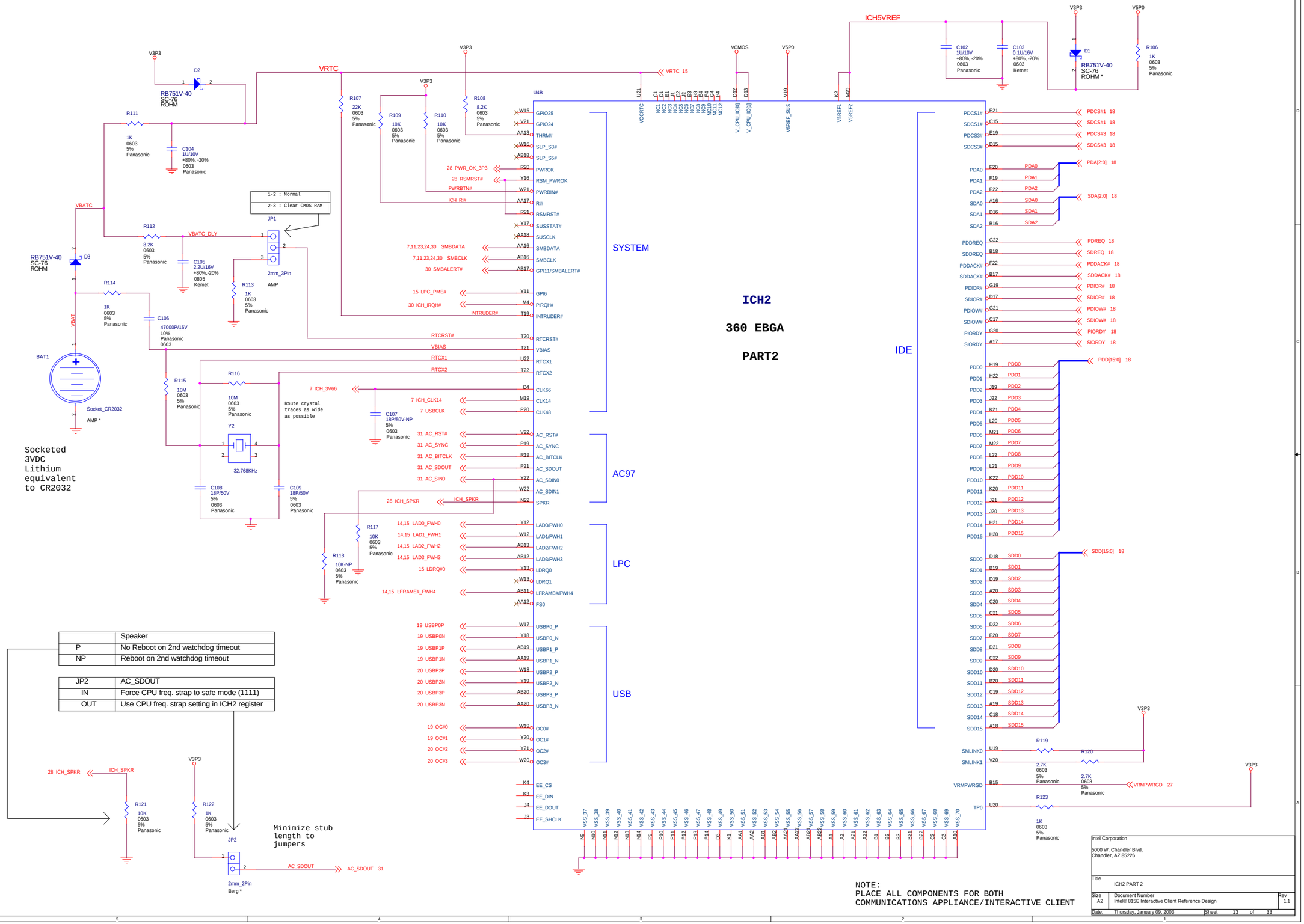
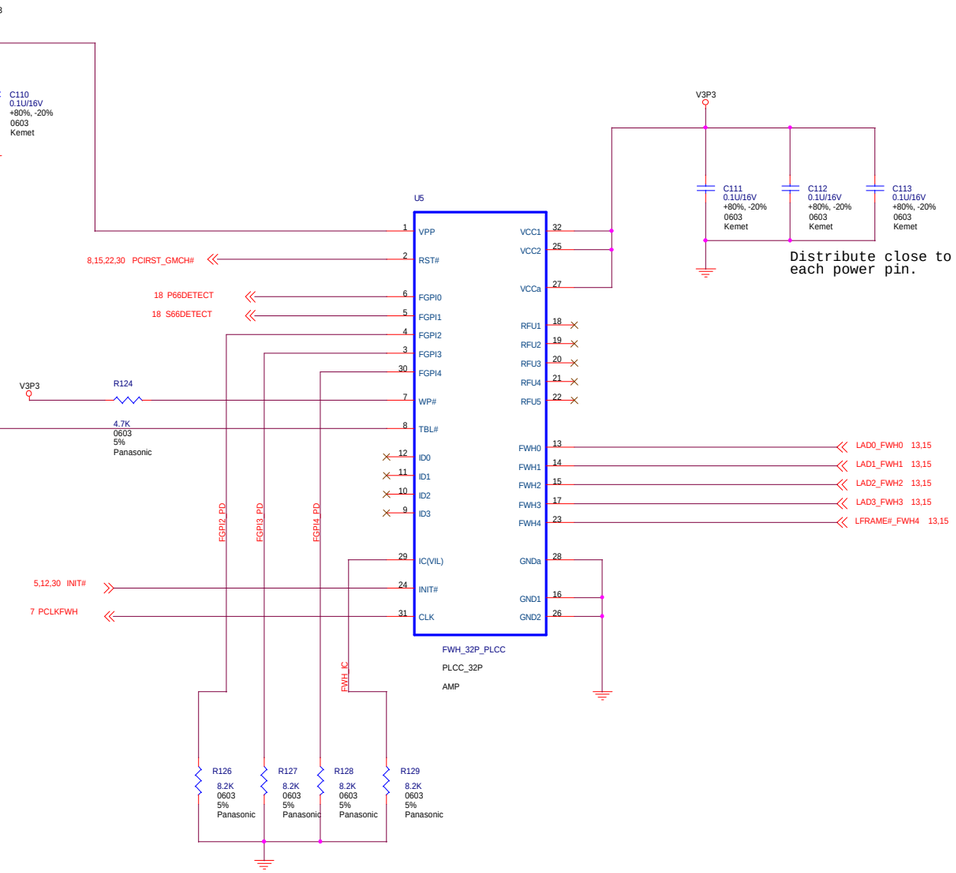


	Speaker
P	No Reboot on 2nd watchdog timeout
NP	Reboot on 2nd watchdog timeout

JP2	AC_SDOUT
IN	Force CPU freq. strap to safe mode (1111)
OUT	Use CPU freq. strap setting in ICH2 register

TOP BLOCK	
IN	Unlocked
OUT	Locked



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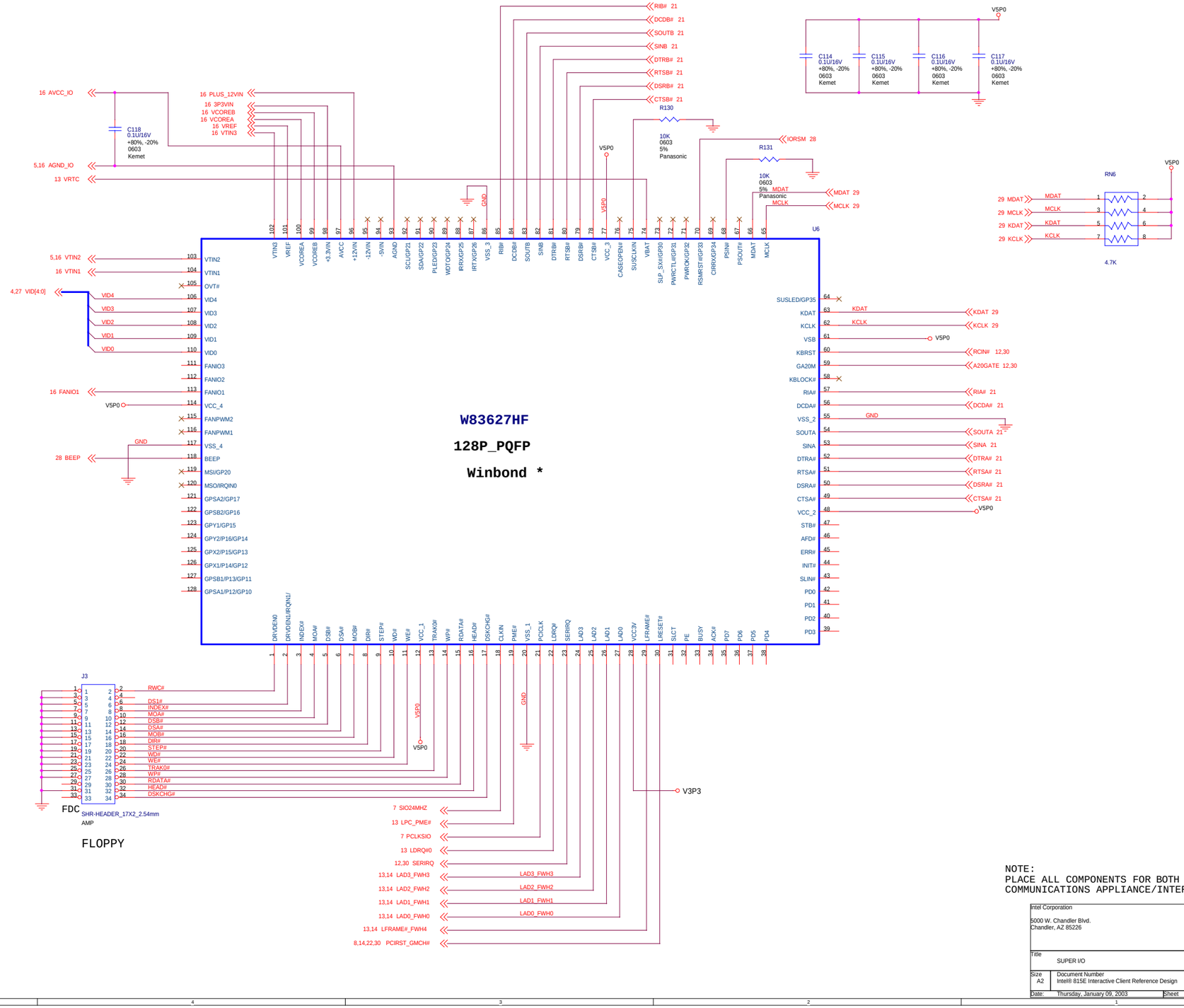
W83627HF
128P_PQFP
Winbond *
U6
J3
FDC
SHR-HEADER_17X2_2.54mm
AMP
FLOPPY
C114 0.1U/16V +80%, -20% 0603 Kemet
C115 0.1U/16V +80%, -20% 0603 Kemet
C116 0.1U/16V +80%, -20% 0603 Kemet
C117 0.1U/16V +80%, -20% 0603 Kemet
C118 0.1U/16V +80%, -20% 0603 Kemet
R130 10K 0603 5% Panasonic
R131 10K 0603 5% Panasonic
RN6 4.7K
V5P0
V3P3
GND
MDAT
MCLK
KDAT
KCLK
VID4
VID3
VID2
VID1
VID0
BEEP
RWC#
DS1#
INDEX#
MOA#
DSB#
DSA#
MOB#
DIR#
STEP#
WD#
WE#
TRAK0#
WP#
RDATA#
HEAD#
DSKCHG#
SUSLED/GP35
KBRST
GA20M
KBLOCK#
RIA#
DCDA#
VSS_2
SOUTA
SINA
DTRA#
RTSA#
DSRA#
CTSA#
VCC_2
STB#
AFD#
ERR#
INIT#
SLIN#
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
ACK#
BUSY
PE
SLCT
LRESET#
LFRAME#
VCC3V
LAD0
LAD1
LAD2
LAD3
SERIRQ
LDRQ#
PCICLK
VSS_1
PME#
CLKIN
DSKCHG#
HEAD#
RDATA#
WP#
TRAK0#
VCC_1
WE#
WD#
STEP#
DIR#
MOB#
DSA#
DSB#
MOA#
INDEX#
DRVDEN1/IRQIN1/
DRVDEN0
NOTE:
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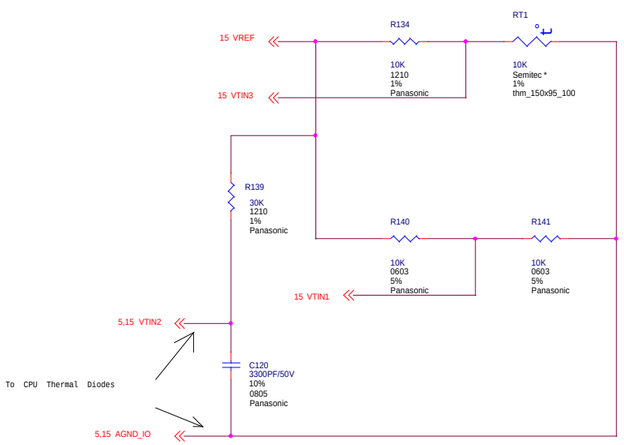
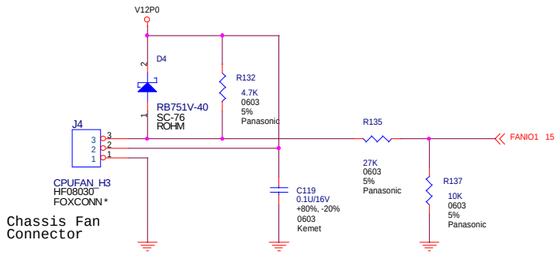
Temperature Sensing

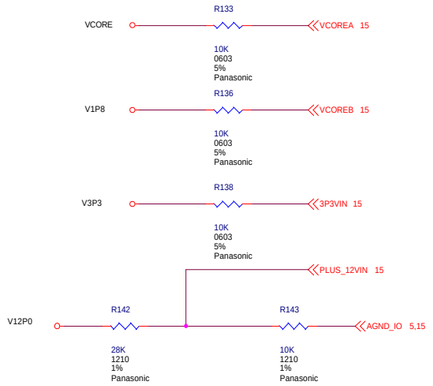


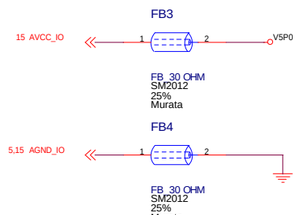
RT1: Sense System Temperature



Chassis Fan Connector

Voltage Sensing





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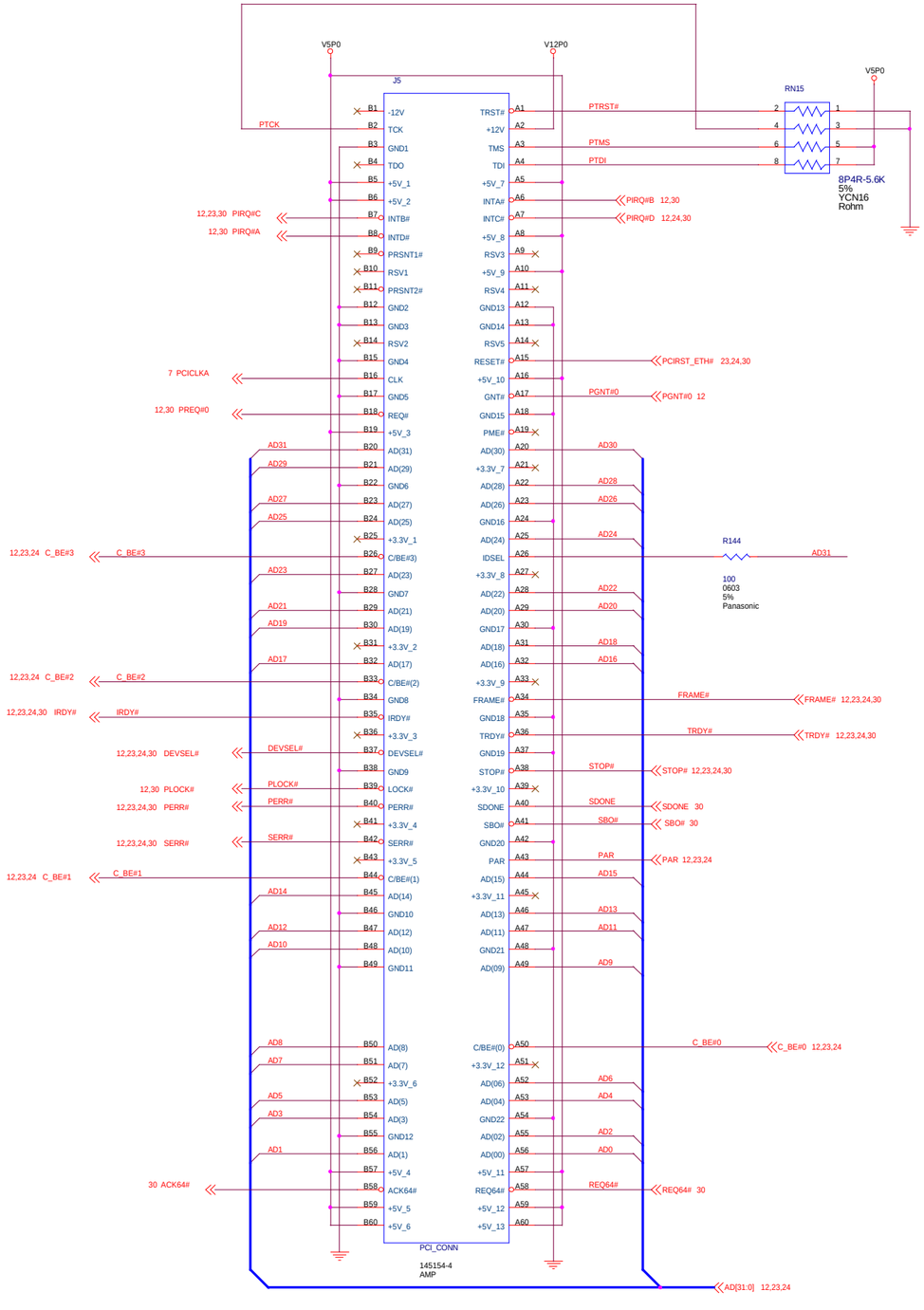

5V PCI CONN., NO 3.3V AND -12V SUPPORT
IDSEL=AD31

NOTE:
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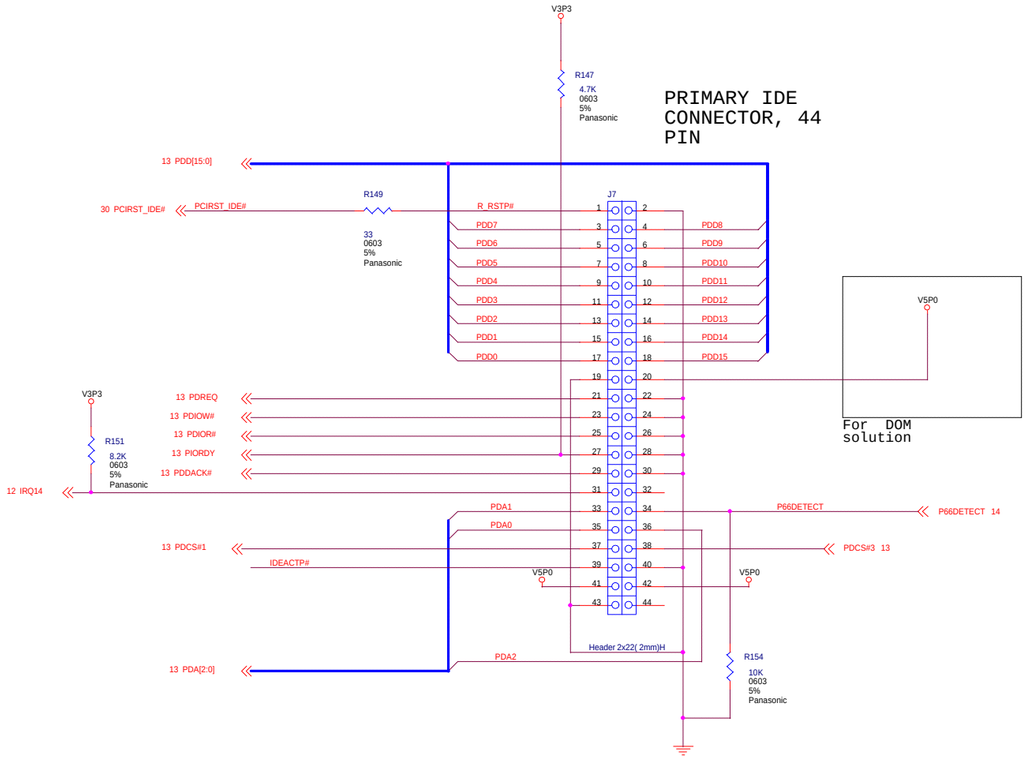

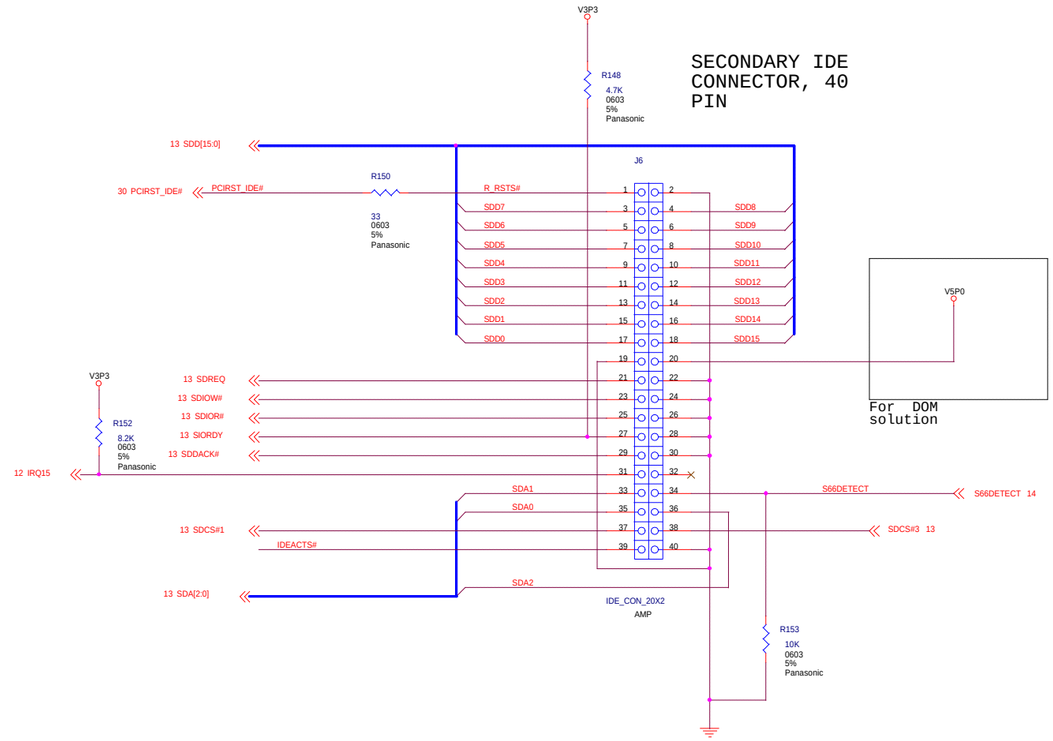

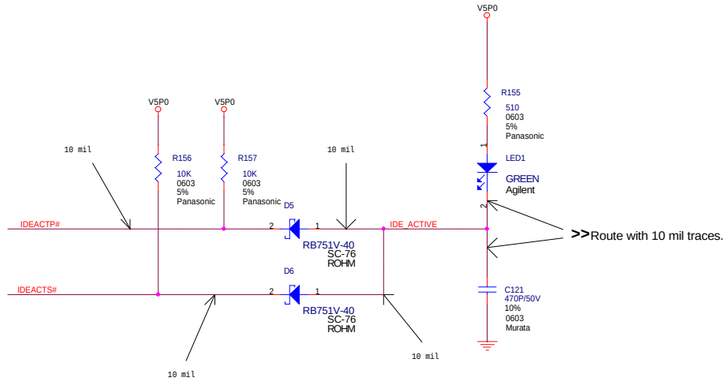

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V5P0

F1
POLYSWITCH 1.25A/15V
Raychem *
SMD125-2

>> Route traces with 60mils at least..

FB5
FB_30 OHM
25%
SM2012
Murata

USB0V5

R158
470K
0603
5%
Panasonic

C122
100U/16V
cp7343
Kemet
20%

C123
470P/50V
5%
0603
Murata

13 OC#0

C124
1000P/50V
10%
0603
Murata

R160
560K
0603
5%
Panasonic

Place within 1" of ICH2

13 USBP0N
13 USBP0P

R159
15
0603
5%
Panasonic

R161
15
0603
5%
Panasonic

C125
47P/50V
5%
0603
Murata

C126
47P/50V
5%
0603
Murata

R162
15K
0603
5%
Panasonic

R163
15K
0603
5%
Panasonic

>> Route traces with 60mils at least..

USBV0
USBD0N
USBD0P

V5P0

F2
POLYSWITCH 1.25A/15V
Raychem
SMD125-2

>> Route traces with 60mils at least.

FB6
FB_30 OHM
25%
SM2012
Murata

USB1V5

R164
470K
0603
5%
Panasonic

C127
100U/16V
cp7343
Kemet
20%

C128
470P/50V
5%
0603
Murata

13 OC#1

C129
1000P/50V
10%
0603
Murata

R166
560K
0603
5%
Panasonic

Place within 1" of ICH2

13 USBP1N
13 USBP1P

R165
15
0603
5%
Panasonic

R167
15
0603
5%
Panasonic

C130
47P/50V
5%
0603
Murata

C131
47P/50V
5%
0603
Murata

R168
15K
0603
5%
Panasonic

R169
15K
0603
5%
Panasonic

>> Route traces with 60mils at least..

USBV1
USBD1N
USBD1P

J8

1 USBV0
2 USBD0N
3 USBD0P
4 USBG0
5 USBV1
6 USBD1N
7 USBD1P
8 USBG1
GND_1 9
GND_2 10
GND_3 11
GND_4 12

DUAL_PORT_USB_CONN.
787745-2
AMP

USBG0
USBG1

C132
47P/50V
5%
0603
Murata

C133
47P/50V
5%
0603
Murata

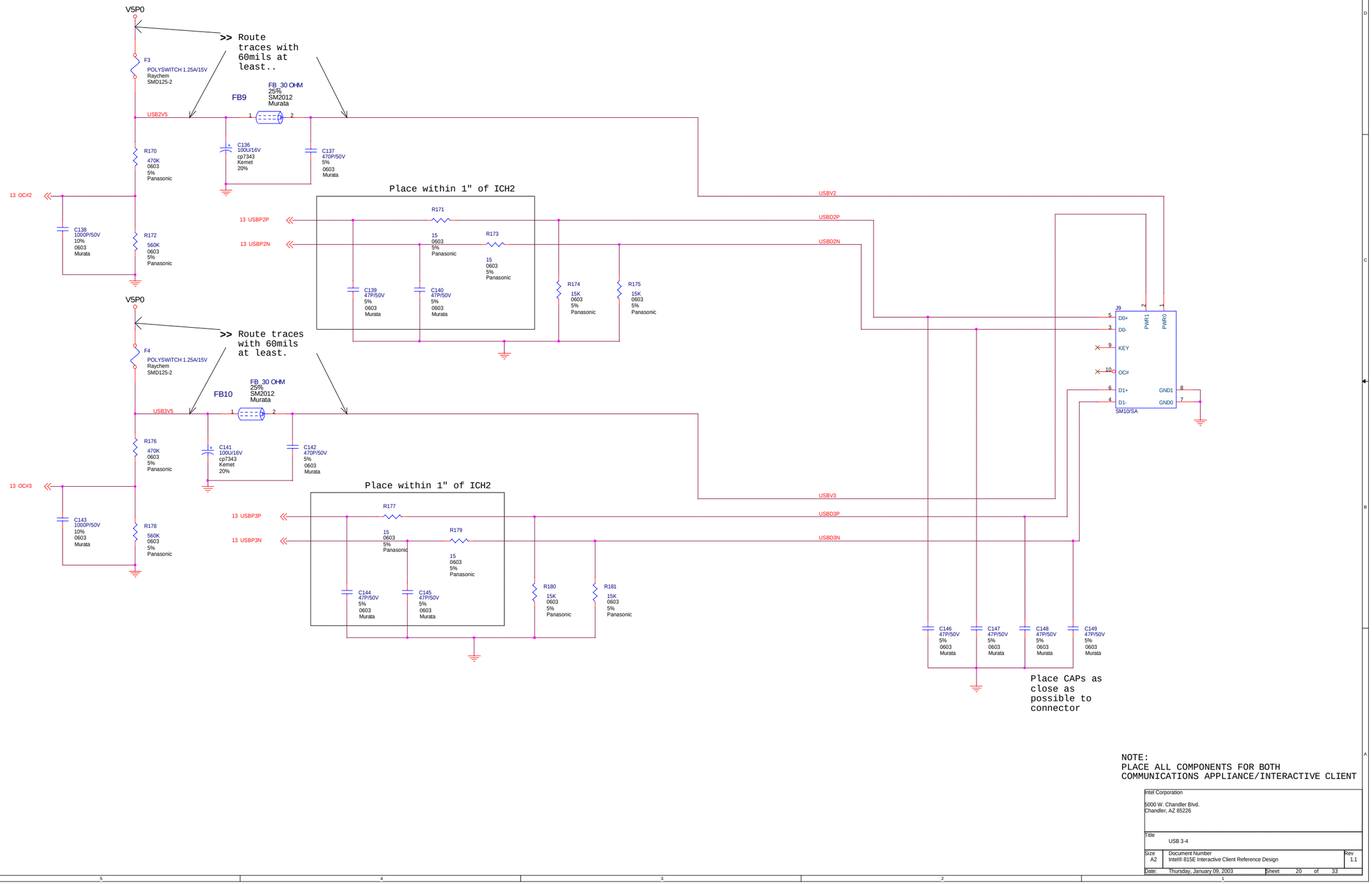
C134
47P/50V
5%
0603
Murata

C135
47P/50V
5%
0603
Murata

Place CAPs as close as possible to connector

NOTE:
PLACE ALL COMPONENTS FOR BOTH
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: USB 1-2		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 19 of 33	


V5P0
>> Route traces with 60mils at least..
F3
POLYSWITCH 1.25A/15V
Raychem
SMD125-2
FB9
FB_30 OHM
25%
SM2012
Murata
USB2V5
R170
470K
0603
5%
Panasonic
C136
100U/16V
cp7343
Kemet
20%
C137
470P/50V
5%
0603
Murata
13 OC#2
C138
1000P/50V
10%
0603
Murata
R172
560K
0603
5%
Panasonic
Place within 1" of ICH2
13 USBP2P
13 USBP2N
R171
15
0603
5%
Panasonic
R173
15
0603
5%
Panasonic
C139
47P/50V
5%
0603
Murata
C140
47P/50V
5%
0603
Murata
R174
15K
0603
5%
Panasonic
R175
15K
0603
5%
Panasonic
USBV2
USBD2P
USBD2N
V5P0
>> Route traces with 60mils at least.
F4
POLYSWITCH 1.25A/15V
Raychem
SMD125-2
FB10
FB_30 OHM
25%
SM2012
Murata
USB3V5
R176
470K
0603
5%
Panasonic
C141
100U/16V
cp7343
Kemet
20%
C142
470P/50V
5%
0603
Murata
13 OC#3
C143
1000P/50V
10%
0603
Murata
R178
560K
0603
5%
Panasonic
Place within 1" of ICH2
13 USBP3P
13 USBP3N
R177
15
0603
5%
Panasonic
R179
15
0603
5%
Panasonic
C144
47P/50V
5%
0603
Murata
C145
47P/50V
5%
0603
Murata
R180
15K
0603
5%
Panasonic
R181
15K
0603
5%
Panasonic
USBV3
USBD3P
USBD3N
J9
D0+
D0-
KEY
OC#
D1+
D1-
PWR1
PWR0
GND1
GND0
SM10/SA
C146
47P/50V
5%
0603
Murata
C147
47P/50V
5%
0603
Murata
C148
47P/50V
5%
0603
Murata
C149
47P/50V
5%
0603
Murata
Place CAPs as close as possible to connector
NOTE:
PLACE ALL COMPONENTS FOR BOTH
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT
Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226
Title
USB 3-4
Size
A2
Document Number
Intel® 815E Interactive Client Reference Design
Rev
1.1
Date: Thursday, January 09, 2003
Sheet 20 of 33

RING INDICATOR SELECT	
1-2	RI Disconnected, External 12 V
2-3	RI Connected (Default)

V12P0

F5
POLYSWITCH 1.50A/15V
Raychem
SMD150-2

JP4

V5P0

R182
10K
0603
5%
Panasonic

U7 ADM213E

15 RTSB#	6	T2IN	T2OUT 3
15 DTRB#	7	T1IN	T1OUT 2
15 SOUTB	20	T3IN	T3OUT 1
	21	T4IN	T4OUT 28
15 RIB#	5	R2OUT	R2IN 4
15 CTSB#	8	R1OUT	R1IN 9
15 DSRB#	19	R5OUT	R5IN 18
15 SINB	26	R3OUT	R3IN 27
15 DCDB#	22	R4OUT	R4IN 23
	13	V+	C1+ 12
	17	V-	C1- 14
			C2+ 15
			C2- 16
	24	EN	
	25	SD#	
	11	VCC	
	10	GND	

RTS#1
DTR#1
TXD#1
RI#1_IN
CTS#1
DSR#1
RXD#1
DCD#1

V5P0 C150 0.1U/16V +80%, -20% Kemet 0603

C161 0.1U/16V +80%, -20% 0603 Kemet

C155 0.1U/16V +80%, -20% 0603 Kemet

C156 0.1U/16V +80%, -20% 0603 Kemet

C151 100P/50V 5% 0603 BC Components

C152 100P/50V 5% 0603 BC Components

C153 100P/50V 5% 0603 BC Components

C154 100P/50V 5% 0603 BC Components

C157 100P/50V 5% 0603 BC Components

C158 100P/50V 5% 0603 BC Components

C159 100P/50V 5% 0603 BC Components

C160 100P/50V 5% 0603 BC Components

Place Close to Header

R1#1
DTR#1
CTS#1
TXD#1
RTS#1
RXD#1
DSR#1
DCD#1

J10B M3 M4 STACKED_DB15_DB9

RING INDICATOR SELECT	
1-2	RI Disconnected, External 12 V
2-3	RI Connected (Default)

V12P0

F6
POLYSWITCH 1.50A/15V
Raychem
SMD150-2

JP5

V5P0

R183
10K
0603
5%
Panasonic

U8 ADM213E

15 RTSA#	6	T2IN	T2OUT 3
15 DTRA#	7	T1IN	T1OUT 2
15 SOUTA	20	T3IN	T3OUT 1
	21	T4IN	T4OUT 28
15 RIA#	5	R2OUT	R2IN 4
15 CTSA#	8	R1OUT	R1IN 9
15 DSRA#	19	R5OUT	R5IN 18
15 SINA	26	R3OUT	R3IN 27
15 DCDA#	22	R4OUT	R4IN 23
	13	V+	C1+ 12
	17	V-	C1- 14
			C2+ 15
			C2- 16
	24	EN	
	25	SD#	
	11	VCC	
	10	GND	

RTS#2
DTR#2
TXD#2
RI#2_IN
CTS#2
DSR#2
RXD#2
DCD#2

V5P0 C162 0.1U/16V +80%, -20% Kemet 0603

C173 0.1U/16V +80%, -20% 0603 Kemet

C167 0.1U/16V +80%, -20% 0603 Kemet

C168 0.1U/16V +80%, -20% 0603 Kemet

C163 100P/50V 5% 0603 BC Components

C164 100P/50V 5% 0603 BC Components

C165 100P/50V 5% 0603 BC Components

C166 100P/50V 5% 0603 BC Components

C169 100P/50V 5% 0603 BC Components

C170 100P/50V 5% 0603 BC Components

C171 100P/50V 5% 0603 BC Components

C172 100P/50V 5% 0603 BC Components

Place Close to Header

DCD#2
RXD#2
TXD#2
DTR#2

J11

1	DCD	DSR	6 DSR#2
2	RX	RTS	7 RTS#2
3	TX	CTS	8 CTS#2
4	DTR	RI	9 RI#2
5	SG	NC	10

SHR_HEADER_5X2_2.54mm
Samtec

NOTE:
PLACE ALL COMPONENTS FOR BOTH
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226

Title: SERIAL PORTS

Size	Document Number	Rev
A2	Intel® 815E Interactive Client Reference Design	1.1

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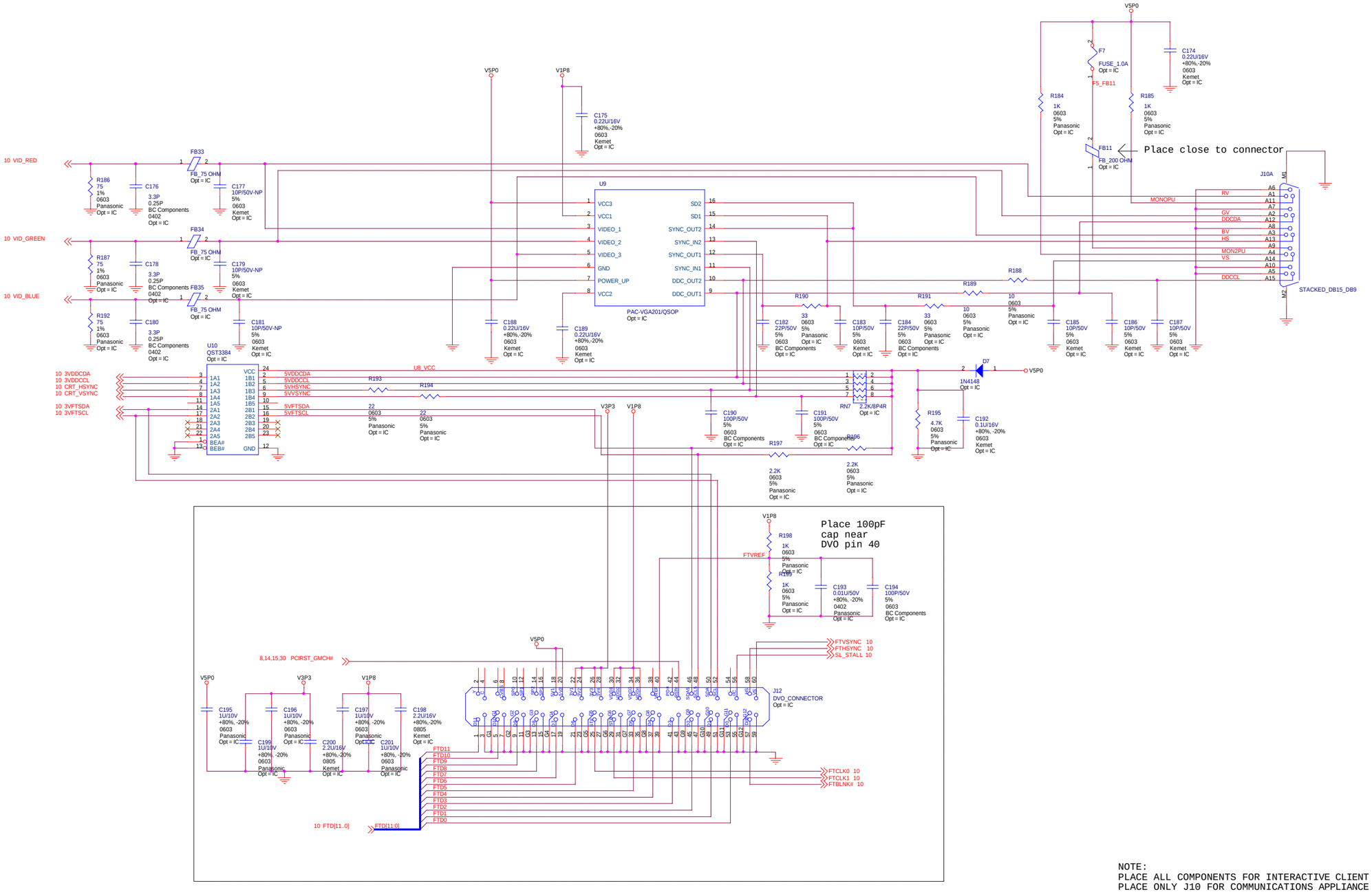


NOTE:
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT
PLACE ONLY J10 FOR COMMUNICATIONS APPLIANCE

Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: VGA AND DVO CONNECTORS		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 22 of 33	

FW82551ER

196_BGA

Intel

LAN Decoupling
Distribute around power pins close to 82551ER.

Close to Ball A10

>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.

>> Trace lengths between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.

>> Trace lengths between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.

>> Trace must be routed directly over a GND plane.

>> Do not route any other traces under the clock circuitry.

Route with 30~50 mils to minimize EMI issues and increase product robustness.

IDSEL = AD29

NOTE:
PLACE ALL COMPONENTS FOR BOTH COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: ETHERNET 1		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 23 of 33	

FW82551ER

196_BGA

Intel

LAN Decoupling
Distribute around power pins close to 82551ER.

V3P3

C215 0.1U/16V +80%, -20% 0603 Kemet Opt = CA
C216 0.1U/16V +80%, -20% 0603 Kemet Opt = CA
C217 0.1U/16V +80%, -20% 0603 Kemet Opt = CA
C218 0.1U/16V +80%, -20% 0603 Kemet Opt = CA

V3P3

C219 0.1U/16V +80%, -20% 0603 Kemet Opt = CA
C220 0.1U/16V +80%, -20% 0603 Kemet Opt = CA
C221 0.1U/16V +80%, -20% 0603 Kemet Opt = CA
C222 0.1U/16V +80%, -20% 0603 Kemet Opt = CA

V3P3

Close to Ball A10

C223 4.7U/10V +80%, -20% 0805 Panasonic Opt = CA
C224 4.7U/10V +80%, -20% 0805 Panasonic Opt = CA

V3P3 pins: G13, K13, N8, P12, A11, A3, A7, E1, K3, N6, P2, E12, G5, G6, H5, H6, H7, H8, J5, J6, J7, J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, K11, L4, L5, L9, L10

12,17,23 AD[31:0]

AD0 N7, AD1 M7, AD2 P6, AD3 P5, AD4 N5, AD5 M5, AD6 P4, AD7 N4, AD8 P3, AD9 N3, AD10 N2, AD11 M1, AD12 M2, AD13 M3, AD14 L1, AD15 L2, AD16 K1, AD17 E3, AD18 D1, AD19 D2, AD20 D3, AD21 C1, AD22 B1, AD23 B2, AD24 B4, AD25 A5, AD26 B5, AD27 B6, AD28 C6, AD29 C7, AD30 A8, AD31 B8

12,17,23 C_BE#[3:0]

C_BE#0 M4, C_BE#1 L3, C_BE#2 F3, C_BE#3 C4

12,17,23,30 FRAME# F2
12,17,23,30 IRDY# F1
12,17,23,30 TRDY# G3
12,17,23,30 DEVSEL# H3
12,17,23,30 STOP# H1
12,17,23 PAR J1
12,17,30 PIRQ#D H2
12,17,23,30 PERR# J2
12,17,23,30 SERR# A2

12,17,23 AD30 — R213 100 0603 5% Panasonic Opt = CA — A4 IDSEL

12,30 PREQ#2 C3
12 PGNT#2 J3
17,23,30 PCIRST_ETH# C2
7 PCLK559B G1

V5P0 — R215 100K 0603 5% Panasonic Opt = CA
V3P3 — 23,28 PWR_OK_LAN B9, ALTRST# A9

7,11,13,23,30 SMBCLK A10
7,11,13,23,30 SMBDATA C9

G2 VIO

LAN2_XTAL1 N11 X1
LAN2_XTAL2 P11 X2

Y4 25MHz 30PPM HC-49/US Fox Opt = CA
C225 22P/50V 5% 0603 BC Components Opt = CA
C226 22P/50V 5% 0603 BC Components Opt = CA
C227 0.1U/16V +80%, -20% 0603 Kemet Opt = CA

Route with 30~50 mils to minimize EMI issues and increase product robustness.

>> Trace lengths between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.

>> Trace lengths between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.

>> Trace must be routed directly over a GND plane.

>> Do not route any other traces under the clock circuitry.

VSPLL[0] G14, VSPLL[1] K12, VSPLL[2] P8, VSPLL[3] N12
VSPT C10
VSPP[0] B3, VSPP[1] B7, VSPP[2] E2, VSPP[3] K2, VSPP[4] M6, VSPP[5] N1
VS[0] D4, VS[1] D5, VS[2] D6, VS[3] D7, VS[4] D8, VS[5] D11, VS[6] E4, VS[7] E5, VS[8] E6, VS[9] E7, VS[10] E8, VS[11] E9, VS[12] E10, VS[13] E11, VS[14] F4, VS[15] F5, VS[16] F6, VS[17] F7, VS[18] F8, VS[19] F9, VS[20] F10, VS[21] F11, VS[22] G7, VS[23] G8, VS[24] G9, VS[25] G10, VS[26] G11, VS[27] H9, VS[28] H10, VS[29] H11, VS[30] L6, VS[31] L11

Opt = CA

U13

LILED A12, ACTLED C11, SPEEDLED B11, TDP C13, TDN C14, RDP E13, RDN E14
SMBALRT# B10, CSTSCHG C5, PME# A6, FLA0/PCIMODE# J13, FLA1/AUXPWR J12, FLA2 K14, FLA3 L14, FLA4 L13, FLA5 L12, FLA6 M14, FLA7 M13, FLA8/IOCHRDY N14, FLA9/IMRST P13, FLA10/MRING# N13, FLA11/MINT M12, FLA12/MCNTSM# M11, FLA13/EEDI P10, FLA14/EEDO N10, FLA15/EESK M10, FLA16 P9
FLD0 F14, FLD1 F13, FLD2 F12, FLD3 G12, FLD4 H14, FLD5 H13, FLD6 H12, FLD7 J14
EECS P7, FLCS# N9, FLOE# M8, FLWE# M9, CLKRUN# C8, TEST A13, TEXEC D13, TCK D14, TI D12, TO B12, RBIAS10 B14, RBIAS100 B13, VREF C12, NC11 D10, NC10 G4, NC9 A14, NC8 J4, NC7 L7, NC6 P1, NC5 D9, NC4 L8, NC3 P14, NC2 H4, NC1 A1

>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.

ACTLED_2 25
SPEEDLED_2 25
TDP_2 25
TDN_2 25
RDP_2 25
RDN_2 25

U14 93C46 SOP_8P Atmel Opt = CA
V3P3 — VCC 8
EEDI 3 — EEDI_2
EEDO 4 — EEDO_2
EESK 2 — EESK_2
EECS 1 — EECS_2
NC2 7, NC1 6
GND 5

R208 619-NP 0603 1% Panasonic Opt = CA
R209 619-NP 0603 1% Panasonic Opt = CA
R210 62K 0603 5% Panasonic Opt = CA
R211 4.7K 0603 5% Panasonic Opt = CA
R212 549 0603 1% Panasonic Opt = CA
R214 619 0603 1% Panasonic Opt = CA

IDSEL = AD30

NOTE:
NO COMPONENTS PLACED FOR INTERACTIVE CLIENT
PLACE ALL COMPONENTS FOR COMMUNICATIONS APPLIANCE

Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226

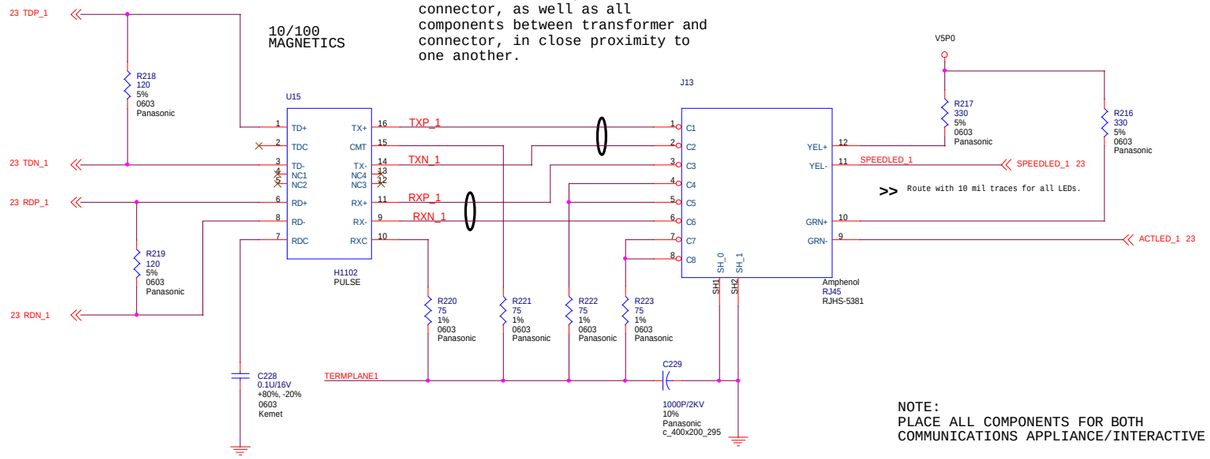
Title: ETHERNET 2

Size: A2 | Document Number: Intel® 815E Interactive Client Reference Design | Rev: 1.1

Date: Thursday, January 09, 2003 | Sheet 24 of 33

ETHERNET 1

>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.
>> Locate transformer, RJ45 connector, as well as all components between transformer and connector, in close proximity to one another.

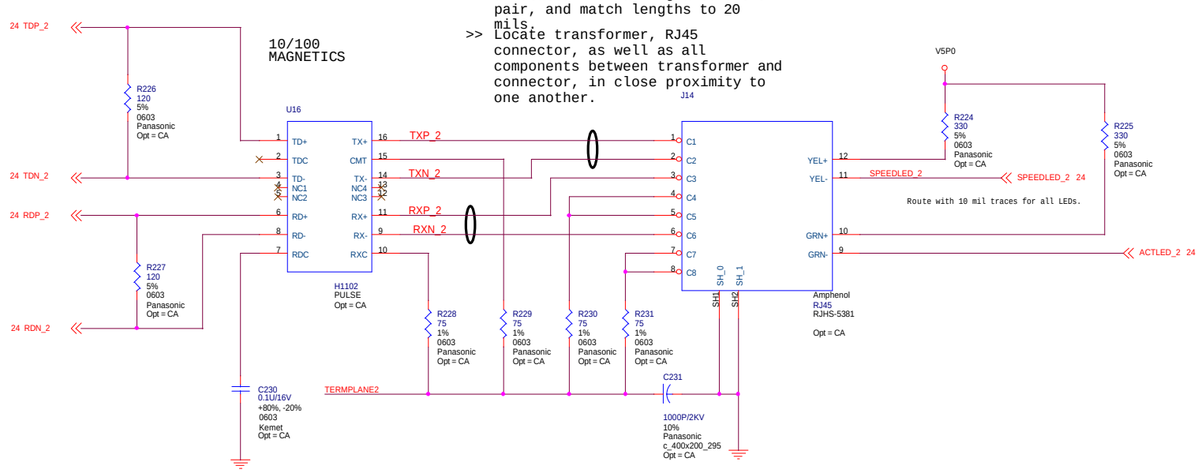


NOTE:
PLACE ALL COMPONENTS FOR BOTH COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

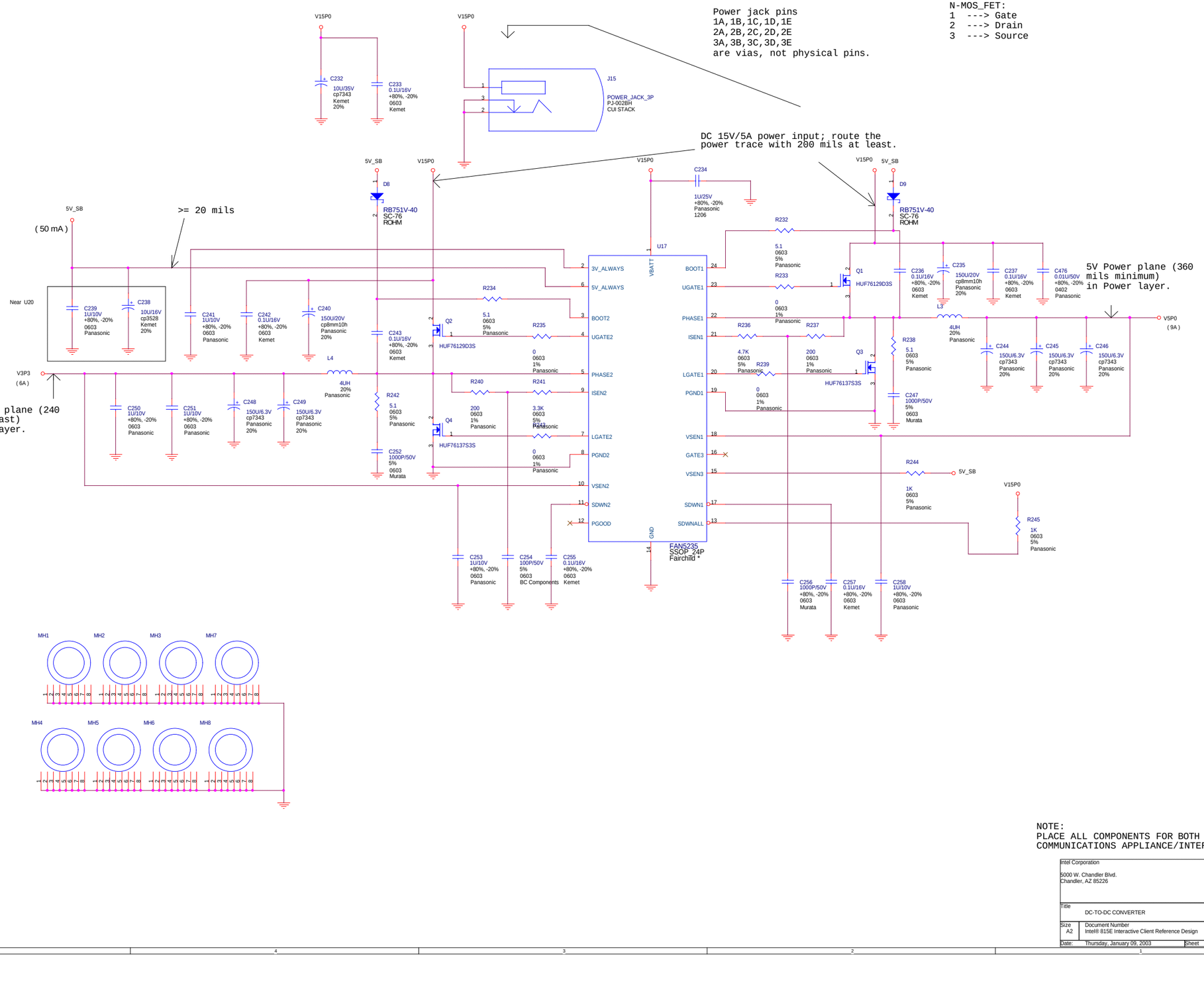
ETHERNET 2

>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.
>> Locate transformer, RJ45 connector, as well as all components between transformer and connector, in close proximity to one another.

NOTE:
PLACE ONLY FOR COMMUNICATIONS APPLIANCE



Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: LAN CONNECTOR		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 25 of 33	



NOTE:
PLACE ALL COMPONENTS FOR BOTH
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

Intel Corporation	
5000 W. Chandler Blvd. Chandler, AZ 85226	
Title	DC-TO-DC CONVERTER
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design — Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 26 of 33

PWM power trace (route as wide as possible)

C259 10U/10V +80%, -20% 1206 Panasonic
C260 10U/10V +80%, -20% 1206 Panasonic
C261 10U/10V +80%, -20% 1206 Panasonic
C262 10U/10V +80%, -20% 1206 Panasonic
C263 10U/10V +80%, -20% 1206 Panasonic
C264 10U/10V +80%, -20% 1206 Panasonic

V5P0

VTT Power Sequencing

R327 10K 0603 5% Panasonic
Float = Forced PWM Mode
C265 0.22U/16V +80%,-20% Kemet 0603
R246 22 5% 0603 Panasonic
Beta = 450
Q19 2N7002
R328 100K 0603 5% Panasonic
Q20 MMBT5089
5 VTTPWRGD
VTTPWRGD

BAT54 D10
C266 1U/10V +80%, -20% 0603 Panasonic
C267 0.1U/16V +80%, -20% Kemet 0603

U18 MAX1813 MAXIM *

VCC	9		
VDD	17		
SKP/SDN#	3	V+	1
ILIM	12	BST	26
REF	11	DH	28
CC	6	LX	27
TIME	4	DL	16
TON	10	VPCS	2
D0	25	PGND	15
D1	24		
D2	23		
D3	22		
D4	21	FB	5
		PGOOD	13
SUS	18	GND	14
S0	7	CODE	20
S1	8	ZMODE	19

Q5 IRF7811
Q6 IRF7811
D11 CMPD2838
D12 CMSH5-40
L5 0.58UH 15% Panasonic

Vcore power island (880 mils minimum) in power layer

VCORE (22A)

C270 220U/2.5V cp7343h Panasonic 20%
C271 220U/2.5V cp7343h Panasonic 20%
C272 220U/2.5V cp7343h Panasonic 20%
C273 220U/2.5V cp7343h Panasonic 20%
C274 220U/2.5V cp7343h Panasonic 20%
C275 220U/2.5V cp7343h Panasonic 20%
C276 10U/10V +80%, -20% 1206 Panasonic

4,15 VID[4:0]
VID0
VID1
VID2
VID3
VID4

R248 1K 5% 0603 Panasonic
R249 1K 5% 0603 Panasonic
R250 1K 5% 0603 Panasonic
R251 1K 5% 0603 Panasonic
R252 1K 5% 0603 Panasonic

C268 0.22U/16V +80%,-20% Kemet 0603
R247 150K 0603 5% Panasonic
C269 47P/50V 5% Murata 0603
R253 51K 0603 5% Panasonic
R254 100 0603 5% Panasonic
R255 0.0015 2512 5% Panasonic
C277 1000P/50V 10% 0603 Murata
R329 0-NP 0603 1% Panasonic

DL gate trace must be short and wide (50-100 mils if MOSFET is 1 inch from IC)

Q7 IRF7822
Q8 IRF7822
Q9 IRF7822

V3P3
R256 100K 0603 5% Panasonic
VRMPWRGD 13

12V Power Trace (200 mils minimum) (5 A)

V15P0
D13 MBRD640CT DPAK ON semiconductor

Pins 6,7,8,9 are vias, not physical Pins.

U19 MIC29512BT TO-220-5_W/Heat_Sink Micrel *

VIN	2	OUT	4
EN	1	ADJ	5
GND	3		

V12P0
R257 2.2K 0603 5% Panasonic
R261 249 0603 1% Panasonic
C284 10U/35V cp5mm5_4h Panasonic 20%
C286 0.1U/25V +80%, -20% Panasonic 0603
C287 10U/35V cp5mm5_4h Panasonic 20%

2.5V Power Trace (20 mils minimum)

U21 MAX1792 MAXIM

IN1	1	OUT1	8
IN2	2	OUT2	7
RST#	3	SET	6
SHDN#	4	GND	5

V3P3
C295 1U/10V +80%, -20% 0603 Panasonic
V2P5
C293 3.3U/10V +80%, -20% AVX 0805
R263 100 0603 1% Panasonic
R264 100 0603 1% Panasonic

PWM power trace (route as wide as possible)

V12P0
C278 0.1U/25V +80%, -20% Panasonic 0603
5V_SB
V5P0

C279 1500U/35V cp16mm16_5h Panasonic 20%
C280 1500U/35V cp16mm16_5h Panasonic 20%
C281 0.1U/16V +80%, -20% Kemet 0603
C282 0.1U/16V +80%, -20% Kemet 0603
C283 0.1U/16V +80%, -20% Kemet 0603

U20 SC1109A Semtech *

VCC	11	STBY	3
BCAP+	4	BST	10
BCAP-	5	DH	9
SS/EN	14	PHASE	7
PGOOD	12	DL	8
VOSENSE	13	GND	6
GATE2	15	GATE1	2
LDOS2	16	LDOS1	1

VTT
R259 1K 5% 0603 Panasonic
5 VTTPWRGD
VTTPWRGD
C285 0.1U/16V +80%, -20% Kemet 0603
C292 0.1U/16V +80%, -20% Kemet 0603

R258 0 1% 0603 Panasonic
R260 2.2 0603 1% KOA
D14 CMPD2838
R262 0 0603 1% Panasonic
Q10 IRLR3103
C475 0.01U/50V +80%, -20% 0402 Panasonic
Q11 IRLR3103
L6 4UH 20% Panasonic

Vtt power island (240 mils minimum)

VTT
C288 1500U/35V cp16mm16_5h Panasonic 20%
C289 1500U/35V cp16mm16_5h Panasonic 20%
C290 1500U/35V cp16mm16_5h Panasonic 20%
C291 0.1U/16V +80%, -20% Kemet 0603

V3P3
C294 330U/2.5V cp8mm6_2h Panasonic 20%
Q12 IRLR3103
VCMOS
C297 330U/2.5V cp8mm6_2h Panasonic 20%
V1P8
Q13 IRLR3103
C296 330U/2.5V cp8mm6_2h Panasonic 20%

NOTE:
PLACE ALL COMPONENTS FOR BOTH COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

Intel Corporation	
5000 W. Chandler Blvd. Chandler, AZ 85226	
Title	IMVP2, VOLTAGE GEN
Size A2	Document Number Intel® 815E Interactive Client Reference Design — Rev 1.1
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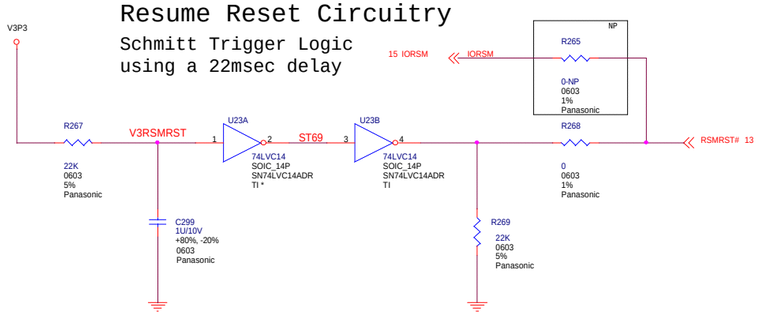
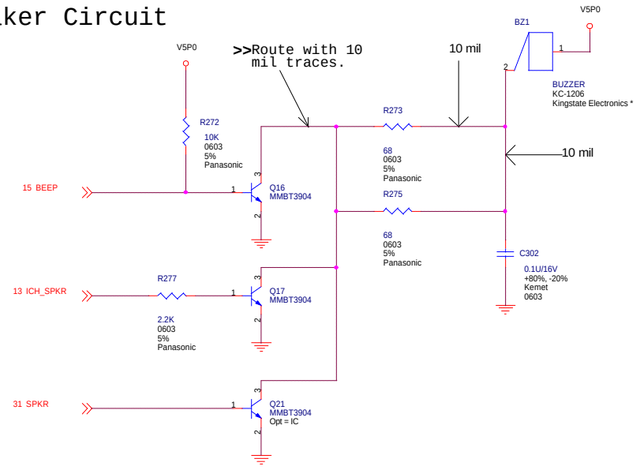
Power Connector and Reset Control

Resume Reset Circuitry

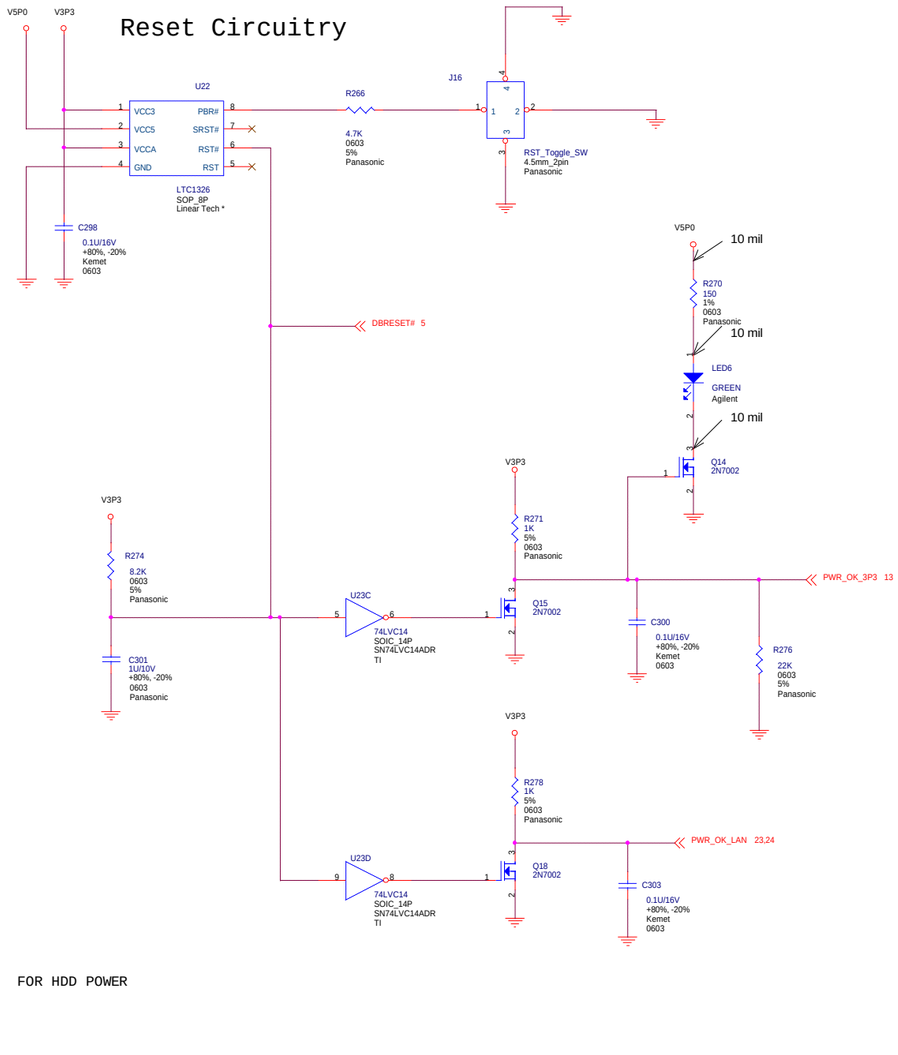
Schmitt Trigger Logic
using a 22msec delay

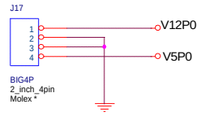


Speaker Circuit



Reset Circuitry

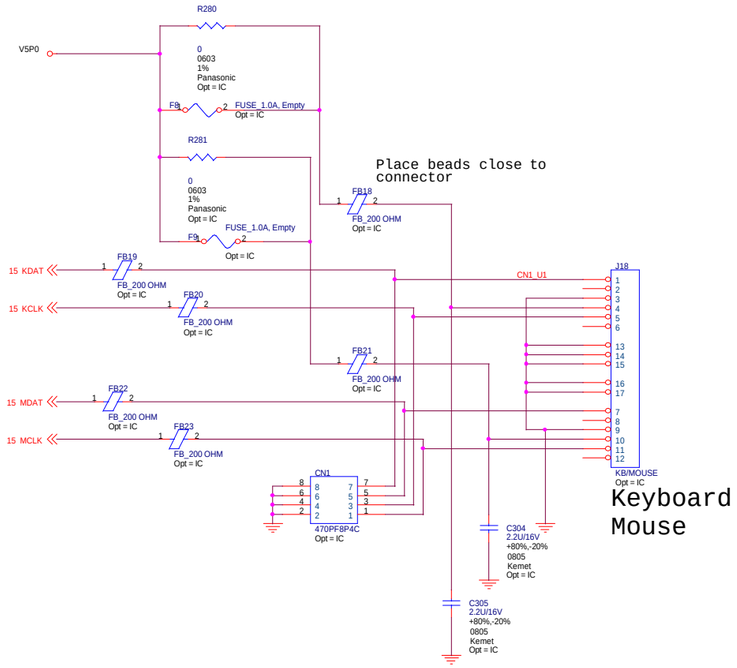




FOR HDD POWER

NOTE:
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT
PLACE ALL BUT Q21 FOR COMMUNICATIONS APPLIANCE

Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: POWER CONNECTOR		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 28 of 33	

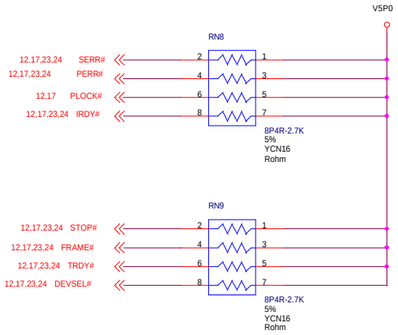


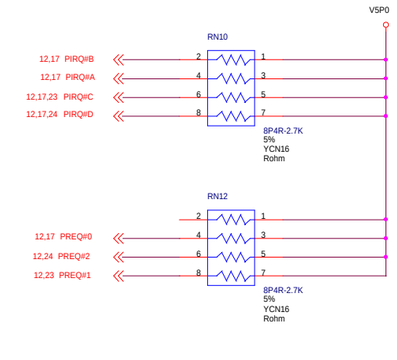
Keyboard Mouse

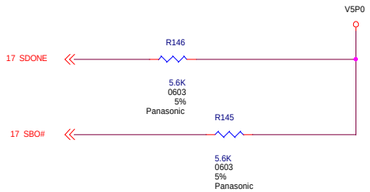
NOTE:
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT
NO COMPONENTS PLACED FOR COMMUNICATIONS APPLIANCE

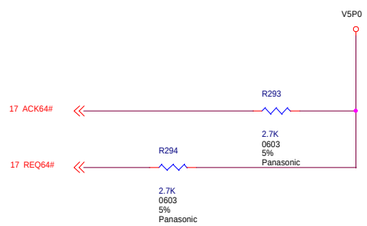
Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: PS/2		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 29 of 33	

PCI BUS

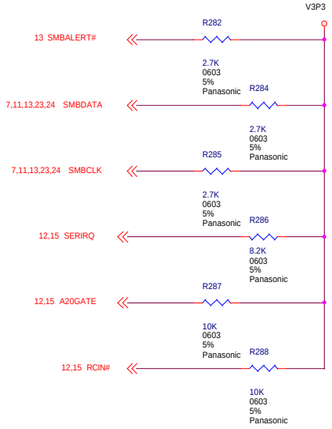


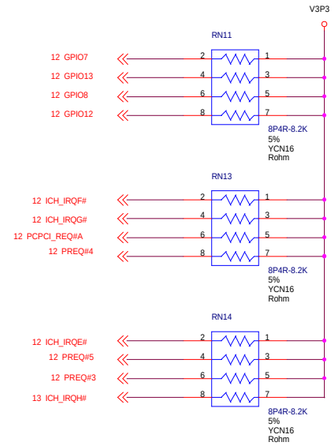






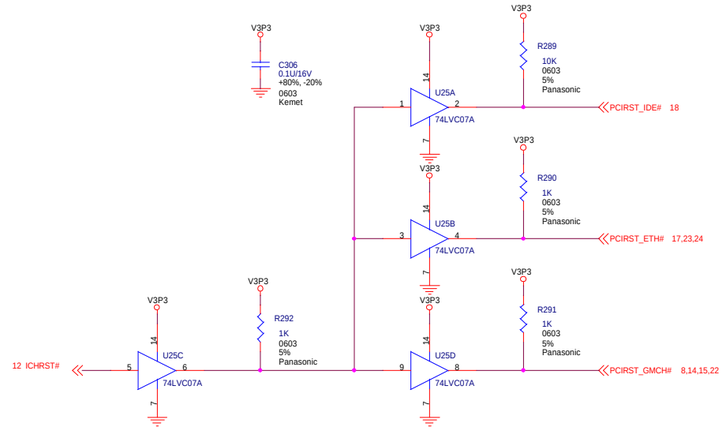
ICH2

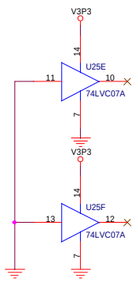




CPU

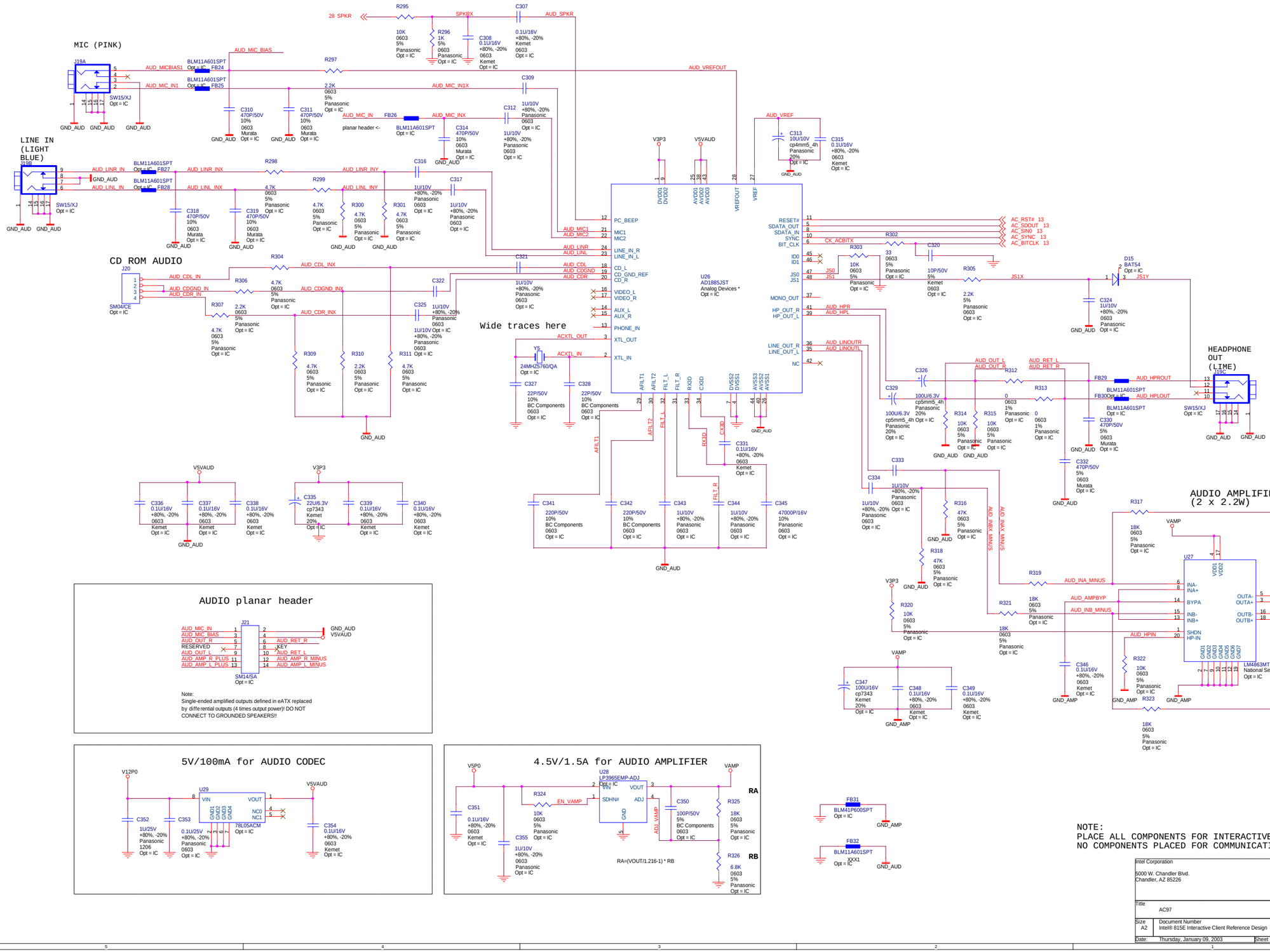
PCIRST# BUFFERING



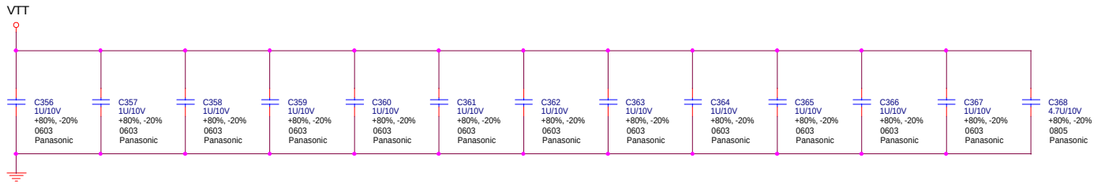


NOTE:
PLACE ALL COMPONENTS FOR BOTH
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

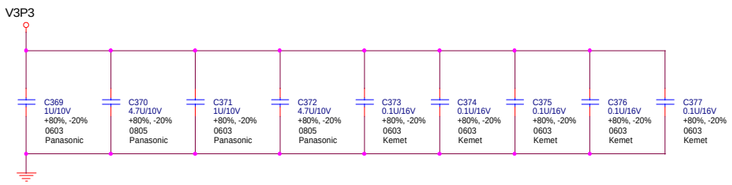
Intel Corporation 5000 W. Chandler Blvd. Chandler, AZ 85226		
Title: Pullup/Pulldown, PCIRST# Buffering		
Size: A2	Document Number: Intel® 815E Interactive Client Reference Design	Rev: 1.1
Date: Thursday, January 09, 2003	Sheet 30 of 33	


MIC (PINK)
J19A
SW15/XJ
Opt = IC
AUD_MIC_BIAS
AUD_MICBIAS1
AUD_MIC_IN1
BLM11A601SPT
FB24
FB25
R297
2.2K
C310 470P/50V 10% 0603 Murata Opt = IC
C311 470P/50V 10% 0603 Murata Opt = IC
AUD_MIC_IN
FB26
planar header <-
AUD_MIC_INX
AUD_MIC_IN1X
C309
C312 1U/10V +80%, -20% Panasonic 0603 Opt = IC
C314 470P/50V 10% 0603 Murata Opt = IC
1U/10V +80%, -20% Panasonic 0603 Opt = IC
LINE IN (LIGHT BLUE)
J19B
AUD_LINR_IN
AUD_LINL_IN
AUD_LINR_INX
AUD_LINL_INX
FB27
FB28
R298
R299
R300
R301
4.7K 0603 5% Panasonic Opt = IC
AUD_LINR_INY
AUD_LINL_INY
C316
C317
1U/10V +80%, -20% Panasonic 0603 Opt = IC
C318 470P/50V 10% 0603 Murata Opt = IC
C319 470P/50V 10% 0603 Murata Opt = IC
CD ROM AUDIO
J20
SM04/CE
Opt = IC
AUD_CDL_IN
AUD_CDGND_IN
AUD_CDR_IN
R304
R306
R307
4.7K 0603 5% Panasonic Opt = IC
2.2K 0603 5% Panasonic Opt = IC
AUD_CDL_INX
AUD_CDGND_INX
AUD_CDR_INX
C321
C322
C325
1U/10V +80%, -20% Panasonic 0603 Opt = IC
R309
R310
R311
2.2K 0603 5% Panasonic Opt = IC
Wide traces here
ACXTL_OUT
ACXTL_IN
Y2
24MHZ5760/QA Opt = IC
C327 22P/50V 10% BC Components 0603 Opt = IC
C328 22P/50V 10% BC Components 0603 Opt = IC
V3P3
V5VAUD
AUD_VREFOUT
AUD_VREF
C313 10U/10V cp4mm5_4h Panasonic 20% Opt = IC
C315 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
U26
AD1885JST
Analog Devices *
Opt = IC
PC_BEEP
MIC1
MIC2
LINE_IN_R
LINE_IN_L
CD_L
CD_GND_REF
CD_R
VIDEO_L
VIDEO_R
AUX_L
AUX_R
PHONE_IN
XTL_OUT
XTL_IN
RESET#
SDATA_OUT
SDATA_IN
SYNC
BIT_CLK
CK_ACBITX
AC_RST# 13
AC_SDOUT 13
AC_SINO 13
AC_SYNC 13
AC_BITCLK 13
R302
R303
33 0603 5% Panasonic Opt = IC
10K 0603 5% Panasonic Opt = IC
C320 10P/50V 5% Kemet 0603 Opt = IC
R305 2.2K 5% Panasonic 0603 Opt = IC
JS1X
D15 BAT54 Opt = IC
JS1Y
C324 1U/10V +80%, -20% 0603 Panasonic Opt = IC
MONO_OUT
HP_OUT_R
HP_OUT_L
AUD_HPR
AUD_HPL
LINE_OUT_R
LINE_OUT_L
AUD_LINOUTR
AUD_LINOUTL
NC
HEADPHONE OUT (LIME)
J19C
SW15/XJ
Opt = IC
AUD_OUT_L
AUD_OUT_R
AUD_RET_L
AUD_RET_R
R312
R313
0 0603 1% Panasonic Opt = IC
FB29
FB30
AUD_HPROUT
AUD_HPLOUT
BLM11A601SPT Opt = IC
C329 100U/6.3V cp5mm5_4h Panasonic 20% Opt = IC
C326
R314 10K 0603 5% Panasonic Opt = IC
R315 10K 0603 5% Panasonic Opt = IC
C330 470P/50V 5% 0603 Murata Opt = IC
C332 470P/50V 5% 0603 Murata Opt = IC
C333
C334 1U/10V +80%, -20% Panasonic 0603 Opt = IC
R316 47K 0603 5% Panasonic Opt = IC
R318 47K 0603 5% Panasonic Opt = IC
AUD_INA_MINUS
AUD_INB_MINUS
AUD_INA_PLUS
AUD_INB_PLUS
AUDIO AMPLIFIER (2 x 2.2W)
R317 18K 0603 5% Panasonic Opt = IC
R319 18K 0603 5% Panasonic Opt = IC
R320 10K 0603 5% Panasonic Opt = IC
R321 18K 0603 5% Panasonic Opt = IC
R322 10K 0603 5% Panasonic Opt = IC
R323 18K 0603 5% Panasonic Opt = IC
U27
INA-
INA+
BYPA
INB-
INB+
SHDN
HP-IN
OUTA-
OUTA+
OUTB-
OUTB+
VDD1
VDD2
GND1
GND2
GND3
GND4
GND5
GND6
GND7
LM4863MTE National Semiconductor * Opt = IC
AUD_AMP_R_MINUS
AUD_AMP_R_PLUS
AUD_AMP_L_MINUS
AUD_AMP_L_PLUS
AUD_HPIN
AUD_AMPBYP
C346 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C347 100U/16V cp7343 Kemet 20% Opt = IC
C348 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C349 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
VAMP
GND_AMP
V5VAUD
V3P3
C336 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C337 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C338 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C335 22U/6.3V cp7343 Kemet 20% Opt = IC
C339 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C340 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C341 220P/50V 10% BC Components 0603 Opt = IC
C342 220P/50V 10% BC Components 0603 Opt = IC
C343 1U/10V +80%, -20% Panasonic 0603 Opt = IC
C344 1U/10V +80%, -20% Panasonic 0603 Opt = IC
C345 47000P/16V 10% Panasonic 0603 Opt = IC
AFILT1
AFILT2
FILT_L
FILT_R
RX3D
CX3D
DVSS2
DVSS1
AVSS3
AVSS2
AVSS1
AUD_MIC1
AUD_MIC2
AUD_LINR
AUD_LINL
AUD_CDL
AUD_CDGND
AUD_CDR
AUD_MIC_INX
AUD_LINR_INX
AUD_LINL_INX
AUD_CDL_INX
AUD_CDGND_INX
AUD_CDR_INX
AUD_MIC_IN1X
AUD_LINR_INY
AUD_LINL_INY
AUD_SPKR
SPKRX
28 SPKR
R295 10K 0603 5% Panasonic Opt = IC
R296 1K 5% 0603 Panasonic Opt = IC
C307 0.1U/16V +80%, -20% 0603 Opt = IC
C308 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
AUD_VREFOUT
AUD_MIC_IN1X
AUD_MIC_INX
AUD_LINR_INY
AUD_LINL_INY
AUD_AMP_R_MINUS
AUD_AMP_R_PLUS
AUD_AMP_L_MINUS
AUD_AMP_L_PLUS
AUD_INA_MINUS
AUD_INA_PLUS
AUD_INB_MINUS
AUD_INB_PLUS
AUDIO planar header
J21
SM14/SA
Opt = IC
AUD_MIC_IN
AUD_MIC_BIAS
AUD_OUT_R
RESERVED
AUD_OUT_L
AUD_AMP_R_PLUS
AUD_AMP_L_PLUS
AUD_RET_R
KEY
AUD_RET_L
AUD_AMP_R_MINUS
AUD_AMP_L_MINUS
GND_AUD
V5VAUD
Note:
Single-ended amplified outputs defined in eATX replaced by diffe rential outputs (4 times output power)! DO NOT CONNECT TO GROUNDED SPEAKERS!!
5V/100mA for AUDIO CODEC
V12P0
U29
VIN
VOUT
NC0
NC1
78L05ACM Opt = IC
C352 1U/25V +80%, -20% Panasonic 1206 Opt = IC
C353 0.1U/25V +80%, -20% Panasonic 0603 Opt = IC
C354 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
4.5V/1.5A for AUDIO AMPLIFIER
V5P0
VAMP
U28
LP3965EMP-ADJ Opt = IC
VIN
VOUT
SDHN#
ADJ
GND
R324 10K 0603 5% Panasonic Opt = IC
EN_VAMP
ADJ_VAMP
C350 100P/50V 5% BC Components 0603 Opt = IC
C351 0.1U/16V +80%, -20% 0603 Kemet Opt = IC
C355 1U/10V +80%, -20% 0603 Panasonic Opt = IC
R325 18K 0603 5% Panasonic Opt = IC
R326 6.8K 0603 5% Panasonic Opt = IC
RA
RB
RA=(VOUT/1.216-1) * RB
FB31
BLM41P600SPT Opt = IC
FB32
BLM11A601SPT Opt = IC
XXX1
NOTE:
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT
NO COMPONENTS PLACED FOR COMMUNICATIONS APPLIANCE
Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226
Title
AC97
Size A2
Document Number
Intel® 815E Interactive Client Reference Design
Rev 1.1
Date: Thursday, January 09, 2003
Sheet 31 of 33

VTT Power Decoupling

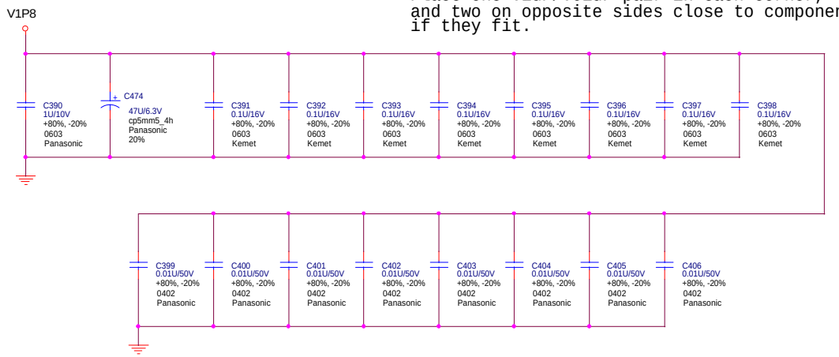


Misc. Power Decoupling



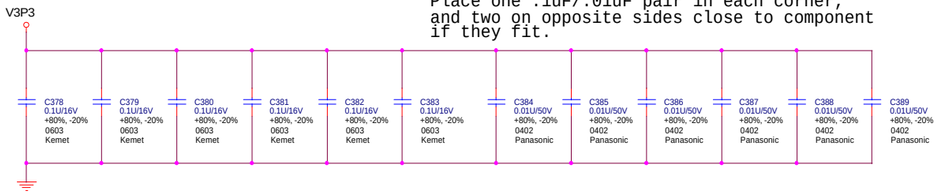
GMCH Decoupling

GMCH Core Plane Decoupling:
Place one .1uF/.01uF pair in each corner,
and two on opposite sides close to component
if they fit.

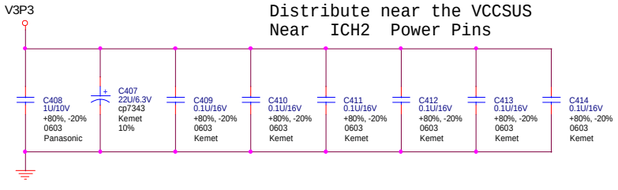


ICH2 Decoupling

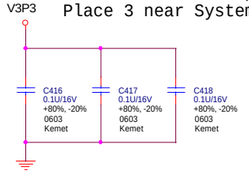
ICH2 3.3V Plane Decoupling:
Place one .1uF/.01uF pair in each corner,
and two on opposite sides close to component
if they fit.

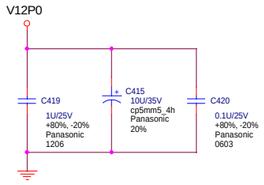


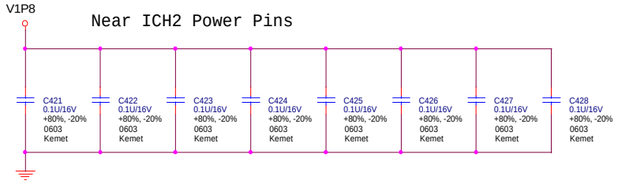
Distribute near the VCCSUS
Near ICH2 Power Pins



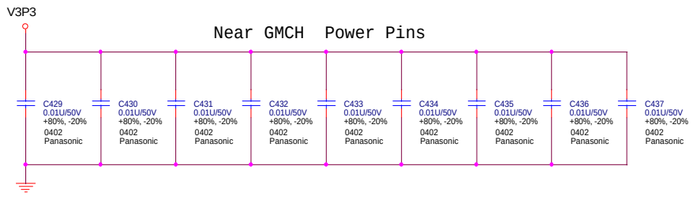
GMCH 3.3V IO Decoupling:
Place 3 near System Memory Quadrant







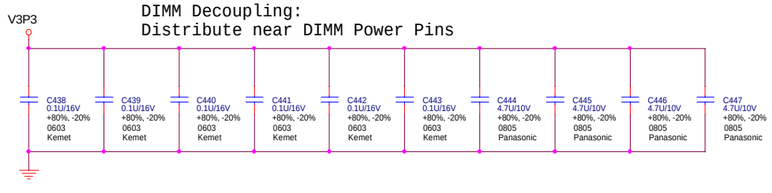
Near ICH2 Power Pins



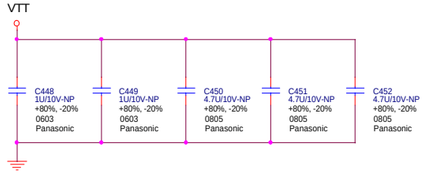
Near GMCH Power Pins

System Memory Decoupling

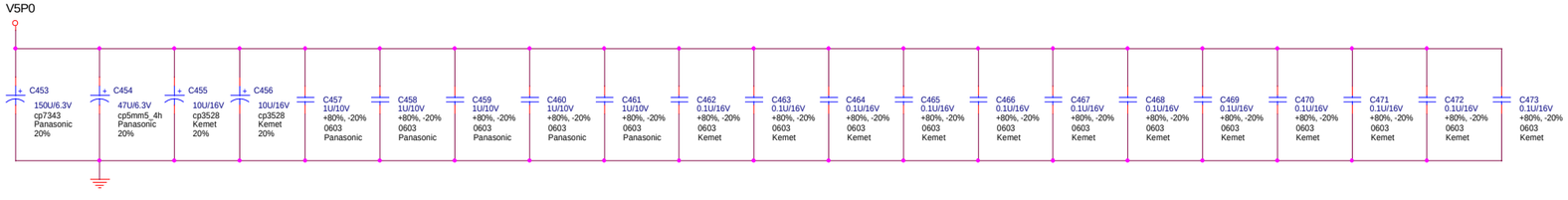
DIMM Decoupling:
Distribute near DIMM Power Pins



VTT Power Decoupling



V5P0 Decoupling



NOTE:
PLACE ALL COMPONENTS FOR BOTH
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

Intel Corporation
5000 W. Chandler Blvd.
Chandler, AZ 85226

Title: DECOUPLING

Size: A2 | Document Number: Intel® 815E Interactive Client Reference Design | Rev: 1.1

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J1: ITP (15x2) Connector

P.N.	Description	P.N.	Description
1	Ground	2	CPURST#
3	Ground	4	DBRESET#
5	Ground	6	TCK
7	TDI	8	TMS
9	TDO	10	VTT
11	TRST#	12	VTT
13	N/C	14	Ground
15	PREQ#	16	Ground
17	PRDY#	18	Ground
19	N/C	20	Ground
21	N/C	22	Ground
23	N/C	24	Ground
25	N/C	26	Ground
27	N/C	28	Ground
29	N/C	30	Ground

J2: VGA Board (6x2) Connector

P.N.	Description	P.N.	Description
1	VID_RED	2	Ground
3	VID_GREEN	4	V1P8
5	VID_BLUE	6	Ground
7	Ground	8	3VDDCDA
9	3VDDCCL	10	CRT_HSYNC
11	CRT_VSYNC	12	V5P0

J3: FDC(17x2) Connector

P.N.	Description	P.N.	Description
1	Ground	2	Density0#
3	Ground	4	N/C
5	Ground	6	Density1#
7	Ground	8	INDEX#
9	Ground	10	MOA#
11	Ground	12	DSB#
13	Ground	14	DSA#
15	Ground	16	MOB#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	WD#
23	Ground	24	WE#
25	Ground	26	TRACK0#
27	Ground	28	WP#
29	N/C	30	RDATA#
31	Ground	32	HEAD#
33	N/C	34	DSKCHG#

J4: Tachometer FAN Connector

Pin Number	Signal Description
1	Ground
2	V12P0
3	Tachometer Signal

J5: PCI BUS CONNECTOR

P.N.	Description	P.N.	Description
B1	N/C	A1	PTRST#
B2	PTCK	A2	V12P0
B3	Ground	A3	PTMS
B4	N/C	A4	PTDI
B5	V5P0	A5	V5P0
B6	V5P0	A6	PIRQ#B
B7	PIRQ#C	A7	PIRQ#D
B8	PIRQ#A	A8	V5P0
B9	N/C	A9	N/C
B10	N/C	A10	V5P0
B11	N/C	A11	N/C
B12	Ground	A12	Ground
B13	Ground	A13	Ground
B14	N/C	A14	N/C
B15	Ground	A15	PCIRST#
B16	PCICLK	A16	V5P0
B17	Ground	A17	PGNT#0
B18	PREQ#0	A18	Ground
B19	V5P0	A19	N/C
B20	AD31	A20	AD30
B21	AD29	A21	N/C
B22	Ground	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	Ground
B25	N/C	A25	AD24
B26	C_BE#3	A26	IDSEL
B27	AD23	A27	N/C
B28	Ground	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	Ground
B31	N/C	A31	AD18
B32	AD17	A32	AD16
B33	C_BE#2	A33	N/C
B34	Ground	A34	FRAME#
B35	IRDY#	A35	Ground
B36	N/C	A36	TRDY#
B37	DEVSEL#	A37	Ground
B38	Ground	A38	STOP#
B39	PLOCK#	A39	N/C
B40	PERR#	A40	SDONE
B41	N/C	A41	SBO#
B42	SERR#	A42	Ground
B43	N/C	A43	PAR
B44	C_BE#1	A44	AD15
B45	AD14	A45	N/C
B46	Ground	A46	AD13
B47	AD12	A47	AD11
B48	AD10	A48	Ground
B49	Ground	A49	AD9
	KEY		KEY
	KEY		KEY
B52	AD8	A52	C_BE#0
B53	AD7	A53	N/C
B54	N/C	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	Ground
B57	Ground	A57	
B58	AD1	A58	AD0
B59	V5P0	A59	V5P0
B60	ACK64#	A60	REQ64#
B61	V5P0	A61	V5P0
B62	V5P0	A62	V5P0

J6, J7: IDE Connectors (Sec=40, Pri=44)

P.N.	Description	P.N.	Description
1	RESET#	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	V5P0
21	DMAREQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Ground
29	DMAACK#	30	Ground
31	IRQ15/14	32	N/C
33	SA1	34	PDIAG#/CSEL
35	SA0	36	SA2
37	HDCCS0#	38	HDCCS1#
39	HDDACTIVE#	40	Ground
41	V3P3	42	V3P3
43	Ground	44	N/C

J8: Dual USB Port Connector

P.N.	Description	P.N.	Description
1	5VP0	5	5VP0
2	USBD0-	6	USBD1-
3	USBD0+	7	USBD1+
4	Ground	8	Ground

J9: Dual USB Header

P.N.	Description	P.N.	Description
1	PWR0	6	D1+
2	PWR1	7	GND0
3	D0-	8	GND1
4	D1-	9	KEY
5	D0+	10	OC#

J10-A: VGA

P.N.	Description	P.N.	Description
1	RV	2	GV
3	BV	4	MON2PU
5	Ground	6	Ground
7	Ground	8	Ground
9	V5P0	10	Ground
11	MONOPU	12	DDCDA
13	HS	14	VS
15	DDCCL		

J10B: Serial Port connector
D-SUB9 Male

Pin Number	Signal Description
1	DCD
2	RXD
3	TXD
4	DTR
5	SGND
6	DSR
7	RTS
8	CTS
9	RI
10	N/C (J1 Only)

J11: Serial Port connector
2x5 Pin Header

Pin Number	Signal Description
1	DCD
2	RXD
3	TXD
4	DTR
5	SGND
6	DSR
7	RTS
8	CTS
9	RI
10	N/C (J1 Only)

J12: DVO Connector

J13, J14: Ethernet RJ45 (8P8C) Connector

P.N.	Description	P.N.	Description
1	TX+	2	TX-
3	RX+	4	Termplane
5	Termplane	6	RX-
7	Termplane	8	Termplane

J15: DC15V/5A Power Jack Connector

Pin Number	Signal Description
1	V15P0
2	Ground
3	Ground

J16: Reset push button (Momentary)

Pin Number	Signal Description
1	Reset signal
2	Ground

J17: Power output connector to HDD

Pin Number	Signal Description
1	V12P0
2	Ground
3	Ground
4	V5P0

J18: KB/Mouse

P.N.	Description	P.N.	Description
1	KDAT	2	N/C
3	Ground	4	Ground
5	KCLK	6	N/C
7	MDAT	8	N/C
9	Ground	10	V5P0
11	MCLK	12	N/C
13	Ground	14	Ground
15	Ground	16	Ground
17	Ground		

J19-A: MIC
J19-B: Line In
J19-C: Headphone Out

J20: CD-ROM Audio

Pin Number	Signal Description
1	Left In
2	Ground In
3	Ground In
4	Right In

J21: Audio Planar

P.N.	Description	P.N.	Description
1	Mic In	2	GND Audio
3	Mic Bias	4	V5VAUD
5	Out Right	6	Ret Right
7	RSVD	8	KEY
9	Out Left	10	Ret Left
11	Amp R+	12	Amp R-
13	Amp L+	14	Amp L-

JUMPER TABLE

JUMPER Ref.	FUNCTION	DEFAULT SETTING
JP1	CLEAR CMOS RAM 1-2 : Normal 2-3 : CLEAR CMOS RAM	1-2 : Normal
JP2	CPU Frequency Strapping IN : Force CPU Frequency to safe mode OUT : Use CPU Frequency strapping in ICH2 Register	OUT : By ICH2 Reg.
JP3	FWH Top Block LOCK IN : TOP BLOCK UNLOCK OUT : TOP BLOCK LOCK	IN : UNLOCK
JP4	Ring Indicator Select 1-2 : RI Disconnected, External 12 V 2-3 : RI Connected	2-3 : RI Connected
JP5	Ring Indicator Select 1-2 : RI Disconnected, External 12 V 2-3 : RI Connected	2-3 : RI Connected

REVISION HISTORY

VERSION	DESCRIPTION
1.0	Rev. B boards built
1.1	Used PSB resistor strapping instead of BSEL

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5000 W. Chandler Blvd.
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Title: REFERENCE TABLES

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